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# Modeling and Analysis of Novel Multilevel Inverter Topology with Minimum Number of Switching Components

**V. Thiyagarajan[1] and P. Somasundaram[2]**

**Abstract:** This paper proposes a novel single phase symmetrical and asymmetrical type extendable multilevel inverter topology with minimum number of switches. The basic circuit of the proposed inverter topology consist of four dc voltage sources and 10 main switches which synthesize 9-level output voltage during symmetrical operation and 17-level output voltage during asymmetrical operation. The comparison between the proposed topology with conventional and other existing inverter topologies is presented in this paper. The advantages of the proposed inverter topology include minimum switches, less harmonic distortion and minimum switching losses. The performance of the proposed multilevel inverter topology has been analyzed in both symmetrical and asymmetrical conditions. The simulation model is developed using MATLAB/SIMULINK software to verify the performance of the proposed inverter.

**Keywords**: Multilevel inverter, symmetric, asymmetric, THD, on state switches.

## 1 Introduction

Multilevel inverters have been emerged as a possible alternative in the field of high power and high voltage applications. The multilevel inverter synthesizes a staircase output voltage waveform with the help of several low or medium input DC voltage sources and power electronic switches [Gupta and Jain (2012)]. The dc voltage sources can be batteries, photovoltaic, ultra-capacitors or fuel cells [Babaei, Hosseini, Gharehpetian et al. (2007)]. The various advantages of multilevel inverter include low distortion, better harmonic profile, high power quality, reduced dv/dt stresses, smaller filter requirements, minimum switching losses and better electromagnetic interference [Kangarlu, Babaei, and Laali (2012); Babaei (2008); Jayabalan, Jeevarathinam and Sandirasegarane (2017)]. However, the drawback of multilevel inverter topology is it requires greater number of power electronic switches and associated gate driver circuits to achieve higher output levels.

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The common topologies of multilevel inverters are cascaded H-bridge (CHB), diode clamped and capacitor clamped inverters [Rodriguez, Lai and ZhengPeng (2002); Boora, Nami, Zare et al. (2010); Khazraei, Sepahvand, Corzine et al. (2012); Rodriguez, Bernet, Steimer et al. (2010)]. In diode clamped multilevel inverters, diodes are used as a clamping device. They require more number of clamping diodes to achieve higher level of output voltage and hence increases the cost and size. The capacitor clamped multilevel inverter uses capacitors which controls both the real and reactive power flow. The major drawbacks of this inverter topology include need of large number of storage capacitors, large size, requires pre-charging of capacitors, more expensive, high switching losses and poor efficiency. The cascade H-bridge multilevel inverter consists of full H-bridges with independent DC voltage sources which provide zero, positive and negative levels of voltages. The advantages of CHB include robustness and ease of control. The CHB multilevel inverter may be symmetric or asymmetric. During symmetric condition, the values of all DC voltage sources are equal and has the advantage of high modularity. During asymmetric condition, the values of DC voltage sources are different and has less modularity [Kangarlu, Babaei and Sabahi (2013)]. The asymmetric inverters generate higher number of output levels in comparison with the symmetric inverters for the same number of dc voltage sources and power electronic switches. Therefore, the size and cost of the asymmetric inverter is lower than that of symmetric inverter [Babaei, Laali and Bayat (2015)].

Many modulation methods such as pulse width modulation (PWM) and space vector PWM methods [Ajami, Mokhberdoran and Oskuee (2013); Thiyagarajan and Somasundaram (2017); Saeedifard, Iravani and Pou (2009)] are proposed to improve the harmonic spectrum of the output voltage. In recent years, many researchers have introduced different inverter topologies to improve the harmonic spectrum of the output voltage. Many symmetrical and asymmetrical inverter topologies have been presented. However, these topologies do not reduce the number of switching devices and the on-state switches. This paper proposes a novel multilevel inverter with reduced number of power electronic switches. The proposed inverter can operate in both symmetrical and asymmetrical conditions. The concept of the proposed inverter topology and the generalized inverter structure are explained in Section-2. The comparative analysis based on the number of dc sources, number of switches and on-state switches is presented in Section-3. The switches angle calculation for the proposed inverter topology is explained in Section-4. The simulation results of the proposed topology are presented in Section-5. The conclusions are presented in Section-6.

## 2 Proposed multilevel inverter topology

The basic circuit of the proposed multilevel inverter topology is shown in Figure 1. The basic circuit consists of four dc voltage sources and ten switches which synthesizes 9-level output voltage during symmetrical conditions and 17-levels output voltage during asymmetrical conditions. The different levels of output voltage obtained across the load during symmetrical condition is shown in Figure 2. During symmetrical condition, the magnitude of all dc voltage sources is equal to $V_{dc}$. There are different switching combinations are possible to synthesize any required level of output voltage. For example,

the switches ($S_1$, $S_5$, $S_7$) or ($S_4$, $S_6$, $S_{10}$) are turned on to achieve level-1 output voltage during positive cycle. Similarly, the switches ($S_4$, $S_5$, $S_9$) or ($S_2$, $S_6$, $S_7$) are turned on to achieve level-1 output voltage during negative cycle. It is noted that the maximum number of on state switches in the conduction path is 4.

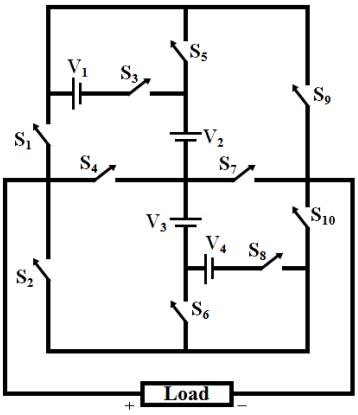
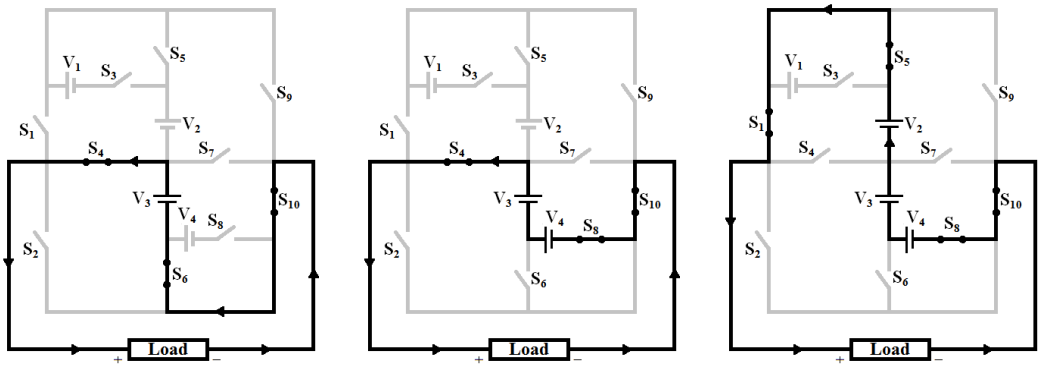
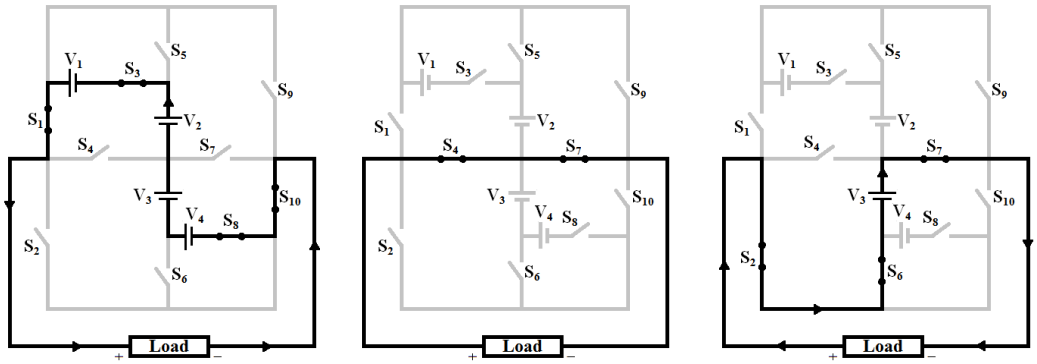


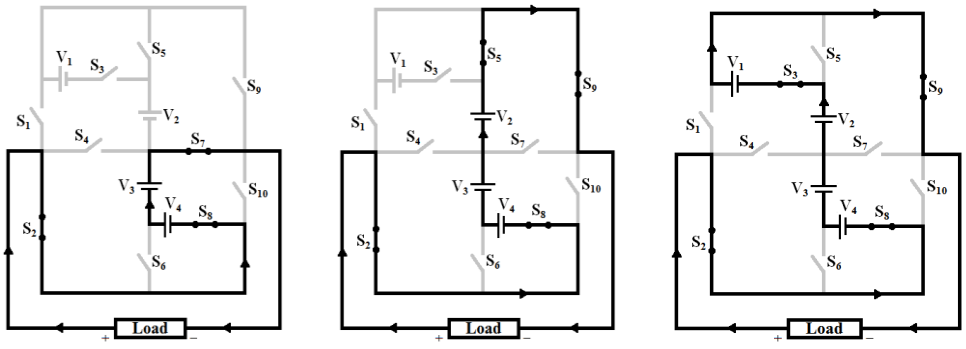

**Figure 1:** Basic circuit of proposed inverter topology




(a) $V_3$ (b) $V_3+V_4$ (c) $V_2+V_3+V_4$




(d) $V_1+V_2+V_3+V_4$ (e) 0 (f) $-V_3$




(g) $-(V_3+V_4)$ (h) $-(V_2+V_3+V_4)$ (i)$-(V_1+V_2+V_3+V_4)$

**Figure 2:** Output voltages during symmetrical condition

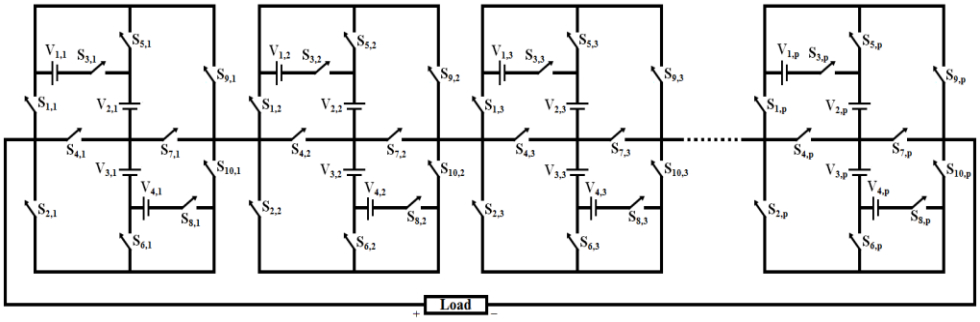



**Figure 3:** General topology of proposed multilevel inverter

The generalized topology of the proposed inverter is shown in Figure 3. Here, 'p' number of basic circuit is connected in series to synthesize the any desired output level. The overall output voltage of the generalized inverter topology is given by,

$$V_o = \sum_{i=1}^{p}\left(V_{1,i}+V_{2,i}+V_{3,i}+V_{4,i}\right) \tag{1}$$

The total number of dc voltage sources in the circuit 'n' is given by,

$$n = 4p \tag{2}$$

The total number of switches 'S' in the generalized inverter topology is given by,

$$S = 10p \tag{3}$$

The relation between 'n' and 'S' is given by,

$$S = \frac{5n}{2} \tag{4}$$

During symmetrical condition, the magnitude of all dc voltage sources is equal to $V_{dc}$. Therefore, the total number of levels 'm' in the output voltage is given by,

$$m = 8p+1 = 2n+1 \tag{5}$$

During asymmetrical condition, the magnitude of dc voltage sources is different and

determined using the following algorithm.
For the first basic circuit with p=1,

$$V_{1,1} = V_{2,1} = V_{dc}$$
$$V_{3,1} = V_{4,1} = 3V_{dc} \quad (6)$$

For the remaining units with p >1,

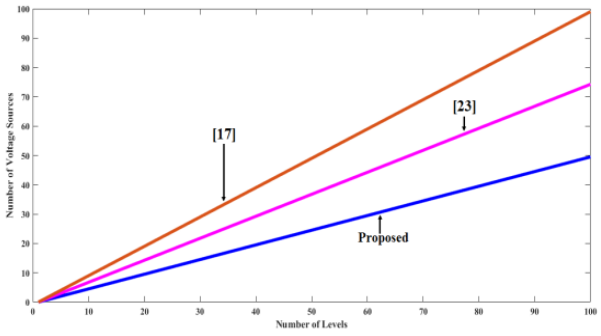
$$V_{1,p} = V_{2,p} = 2\sum_{i=1}^{p-1}\left(V_{1,i} + V_{2,i} + V_{3,i} + V_{4,i}\right) + 1 \quad (7)$$
$$V_{3,p} = V_{4,p} = 3V_{1,p} = 3V_{2,p}$$

Therefore, the total number of levels 'm' in the output voltage during asymmetrical condition is given by,

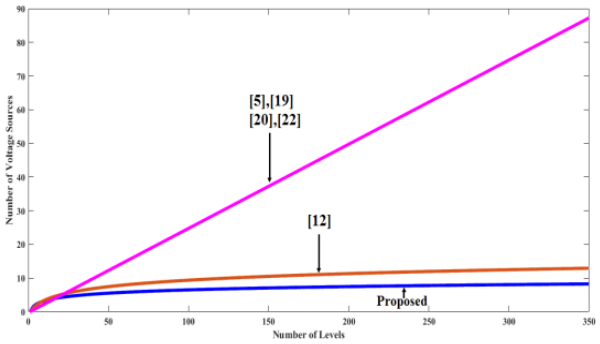
$$m = 17^{p} = 17^{\left(\frac{n}{4}\right)} \quad (8)$$

## 3 Comparison

This sections presents the comparison of the proposed multilevel inverter topology with CHB and other existing topologies. The comparison is done based on the number of dc voltage sources, number of switches and number of on state switches to achieve the required levels in the output voltage. With 'n' dc voltage sources, the proposed inverter topology synthesizes 2n+1 output levels, which is same as that of CHB and other topologies presented in Thamizharasan, Baskaran and Ramkumar et al. (2014); Ajami, Oskuee, Khosroshahi et al. (2014); Prabaharan and Palanisamy (2017). For the proposed inverter topology, the number of dc voltage sources 'n' to achieve 'm' level for the proposed inverter is very less as compared with topologies presented in Lee, Sidorov, Lim et al. (2017); Odeh, Obe and Ojo (2016) during symmetrical condition. The proposed inverter synthesizes $17^{(n/4)}$ levels in the output voltage during asymmetrical condition. However, the topologies presented in Samadaei, Sheikholeslami, Gholamian et al. (2017); Prabaharan and Palanisamy (2017) requires more number of voltage sources to achieve higher levels. The comparison of the number of levels versus number of dc voltage sources during symmetrical and asymmetrical condition are shown in Figure 4 (a) and Figure 4 (b) respectively.



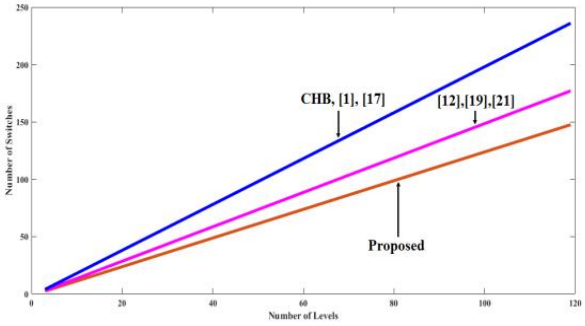

(a) Symmetrical Condition



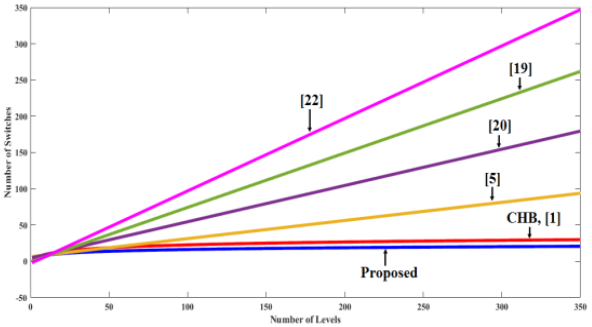

(b) Asymmetrical Condition

**Figure 4:** Levels vs Sources

Figure 5 (a) and (b) shows the plot between the number of levels and switches during symmetrical and asymmetrical conditions respectively. It is seen that the proposed inverter topology uses minimum number of switches to synthesize higher output levels. The proposed topology requires $\frac{5(m-1)}{4}$ switches during symmetrical condition and $10\frac{\log m}{\log 17}$ switches during asymmetrical condition.




(a) Symmetrical Condition




(b) Asymmetrical Condition

**Figure 5:** Level vs Switches

Figure 6 shows the plot between the number of voltage sources and number of on-state switches. The on-state switches are nothing but the switches in the conduction path of the current. For the proposed topology, the maximum number of switches to be turned on to achieve any level is equal to the number of dc voltage sources 'n'. It is seen that the number of switches in the current conduction path of the proposed inverter topology is minimum than that of other existing topologies.

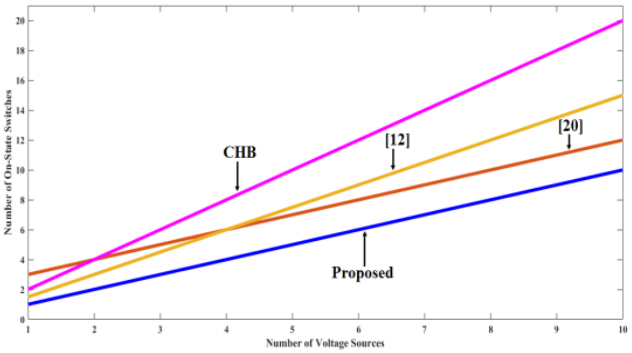



**Figure 6:** On-State Switches

## 4 Switching angle calculation

This section explains the calculation of switching angle for the proposed inverter topology. It plays an important role to reduce the total harmonic distortion (THD). For 'm' level inverter, 2 (m-1) switching angles has to be determined [Luo and Ye (2013)]. An 'm' level inverter has (m-1)/2 main switching angles corresponding to the period $0^o$ to $90^o$. The other switching angles are obtained from the main switching angles using the following relations [Luo and Ye (2013); Thiyagarajan and Somasundaram (2017)]:

1. For period $0^o$ to $90^o$

$=\theta_1, \theta_2, \ldots, \theta_{(m-1)/2}$.

2. For period $90^o$ to $180^o$

$=\theta_{(m+1)/2}. . ., \theta_{(m-1)}. =(\pi-\theta_{(m-1)/2}),. . .,(\pi-\theta_1)$.

3. For period $180^o$ to $270^o$

$=\theta_m, . . ., \theta_{3(m-1)/2} =(\pi+\theta_1),. . .,(\pi+\theta_{(m-1)/2})$.

4. For period $270^o$ to $360^o$

$=\theta_{(3m-1)/2},.. ., \theta_{2(m-1)}=(2\pi- \theta_{(m-1)/2}),...,(2\pi-\theta_1)$.

For the proposed multilevel inverter, the main switching angles are determined using the following equation [Luo and Ye (2013)].

$$\theta_k = \sin^{-1}\left(\frac{2k-1}{m-1}\right), k = 1,2,...,\left(\frac{m-1}{2}\right) \quad (6)$$

The main switching angles for 9-level and 17-level inverter topology are given in Table 1.

**Table 1:** Switching Angles

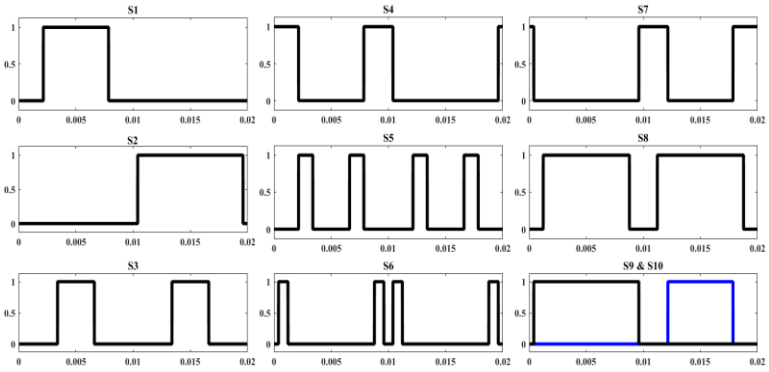
| Level | Switching Angles (in degree) | | | |
|---|---|---|---|---|
| 9-Level | $\theta_1$=7.181 | $\theta_2$=22.024 | $\theta_3$=38.682 | $\theta_4$=61.045 |
| 17-Level | $\theta_1$=3.583 | $\theta_2$=10.807 | $\theta_3$=18.21 | $\theta_4$=25.945 |
| | $\theta_5$=34.229 | $\theta_6$ =43.433 | $\theta_{7=}$54.341 | $\theta_8$=69.636 |

## 5 Simulation results and discussion

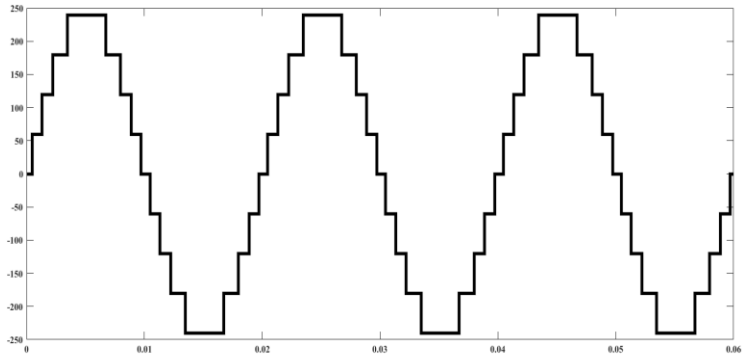
The simulation results are presented in this section. The basic circuit of the proposed inverter topology with four dc voltage sources and 10 switches is considered for the simulation analysis. This topology synthesizes 9-level and 17-level during the symmetrical and asymmetrical conditions respectively. A series RL load with magnitude R=5Ω and L=10mH is considered. A MATLAB / SIMULINK software is used for the simulation analysis.

### *5.1 Symmetric 9-level*

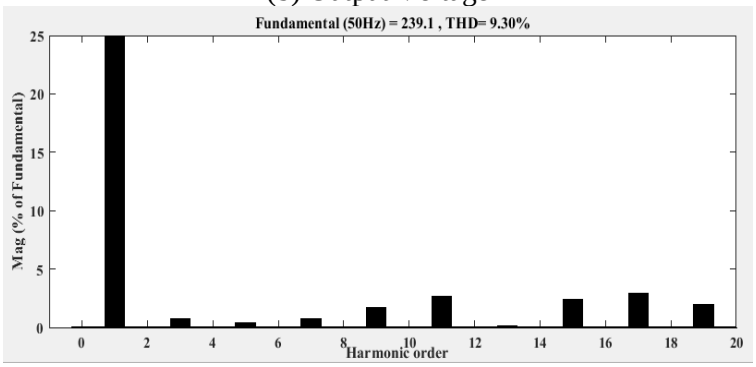
In this case, the magnitude of each dc voltage sources are taken as $V_1$=$V_2$=$V_3$=$V_4$=60 $V_{dc}$. The maximum output voltage obtained across the load is 240 V. The switching pulses, output voltage and its harmonic spectrum for 9-level symmetric operation are shown in Figure 7. The switching states of the inverter topology during symmetrical condition is given in Table 2. It is observed that the THD of the 9-level output voltage waveform is obtained as 9.30%.




(a) Gate pulses



(b) Output Voltage




(c) FFT Analysis

**Figure 7:** Simulation Results during symmetrical condition

**Table 2:** Switching states for 9-level

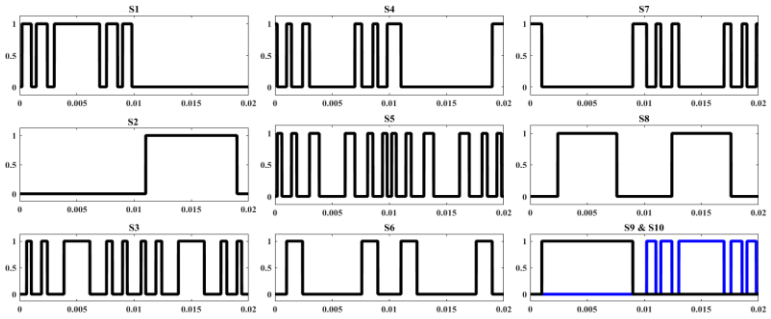
| **Output Voltage** | **$S_1$** | **$S_2$** | **$S_3$** | **$S_4$** | **$S_5$** | **$S_6$** | **$S_7$** | **$S_8$** | **$S_9$** | **$S_{10}$** |
|---|---|---|---|---|---|---|---|---|---|---|
| 4 $V_{dc}$ | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 3 $V_{dc}$ | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 2 $V_{dc}$ | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| $V_{dc}$ | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| -$V_{dc}$ | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| -2 $V_{dc}$ | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| -3 $V_{dc}$ | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| -4 $V_{dc}$ | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

### *5.2 Asymmetric 17-level*

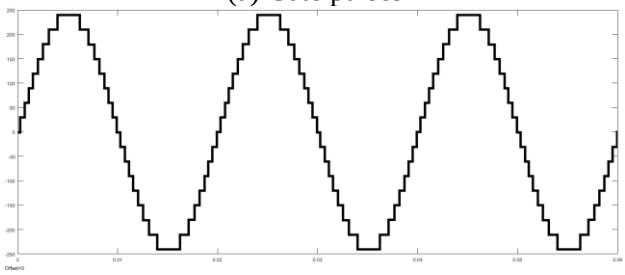
In this case, the magnitude of dc voltage sources is taken as $V_1=V_2=30\ V_{dc}$ and $V_3=V_4=90\ V_{dc}$. The maximum output voltage obtained across the load is 240 V. The switching pulses, output voltage and its harmonic spectrum for 17-level asymmetric operation are shown in Figure 8. The switching states of the inverter topology during asymmetrical condition is given in Table 3. It is observed that the THD of the 9-level output voltage waveform is obtained as 4.87%.

**Table 3:** Switching states for 17-level

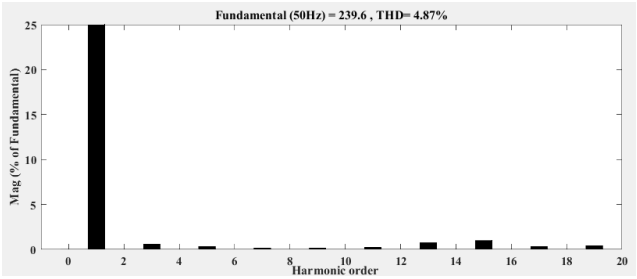
| **Output Voltage** | **$S_1$** | **$S_2$** | **$S_3$** | **$S_4$** | **$S_5$** | **$S_6$** | **$S_7$** | **$S_8$** | **$S_9$** | **$S_{10}$** |
|---|---|---|---|---|---|---|---|---|---|---|
| 8 $V_{dc}$ | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 7 $V_{dc}$ | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 6 $V_{dc}$ | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 5 $V_{dc}$ | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 4 $V_{dc}$ | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 3 $V_{dc}$ | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 2 $V_{dc}$ | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| $V_{dc}$ | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| -$V_{dc}$ | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| -2 $V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| -3 $V_{dc}$ | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| -4 $V_{dc}$ | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| -5 $V_{dc}$ | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| -6 $V_{dc}$ | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| -7 $V_{dc}$ | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| -8 $V_{dc}$ | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |




(a) Gate pulses



(b) Output Voltage




(c) FFT Analysis

**Figure 8:** Simulation Results during asymmetrical condition

## 6 Conclusion

A new extendable multilevel inverter topology is proposed in this paper. The basic circuit of the proposed inverter achieves 9 level output voltage during symmetrical condition and 17 level output voltage during asymmetrical condition. A comparison of the proposed inverter topology with other existing topologies is presented in this paper. The comparative analysis shows that the proposed inverter uses minimum number of components to synthesize larger output levels. The feasibility of the proposed inverter is analyzed using MATLAB software and the result exhibit the good performance of the proposed inverter topology.

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