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Article

Performance Measurement of Energy Efficient and Highly Scalable Hybrid Adder

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Abstract: The adders are the vital arithmetic operation for any arithmetic operations like multiplication, subtraction, and division. Binary number additions are performed by the digital circuit known as the adder. In VLSI (Very Large Scale Integration), the full adder is a basic component as it plays a major role in designing the integrated circuits applications. To minimize the power, various adder designs are implemented and each implemented designs undergo defined drawbacks. The designed adder requires high power when the driving capability is perfect and requires low power when the delay occurred is more. To overcome such issues and to obtain better performance, a novel parallel adder is proposed. The design of adder is initiated with 1 bit and has been extended up to 32 bits so as verify its scalability. This proposed novel parallel adder is attained from the carry look-ahead adder. The merits of this suggested adder are better speed, power consumption and delay, and the capability in driving. Thus designed adders are verified for different supply, delay, power, leakage and its performance is found to be superior to competitive Manchester Carry Chain Adder (MCCA), Carry Look Ahead Adder (CLAA), Carry Select Adder (CSLA), Carry Select Adder (CSA) and other adders.

Keywords: VLSI; full adder; carry look ahead adder; novel parallel adder

1 Introduction

VLSI applications comprises of digital signal processing, image and video processing, microprocessors and microcontrollers, which make extensive consumption of arithmetic operations. In several arithmetic operations, addition, subtraction, multiplication plus accumulation are generally utilized [1]. The most basic arithmetic operation is addition and several adders are utilized in VLSI. Key building block [2] of the Arithmetic and logic unit (ALU) is adder therefore, increasing its effect on speed and decreasing its power consumption will greatly disturb the speed yet power consumption of the processor. Several experiments have been under taken to optimize the speed and power of these units, obviously there is great need to accomplish higher speed at low power consumption, which is a task for designers.

Generally, the rise in speed is reached at the expense of more power consumption of the precision processing unit. Sacrificing the accuracy of the estimation is one of the strategies to enhance both power

and speed. Researchers in the field of approximate calculation pay distinct consideration to adders. The hybrid adder is concentrated in [3], in which it is recommended to use the approximate Reverse Carry Propagation Full Adder (RCPFA), it transmits the input carry in a reverse flow, that is, to begin a carry output starting the higher substantial bit towards lower substantial bit. Due to reverse propagation, the carry weight decreases with the propagation, moreover the adder is less susceptible to delay changes and increase the delay of about 27%. The Lower part OR Adder (LOA) [4], splits the n-bit adder into two sub-adders where, the high significant sub-adder consists of $(n_h - 1)$-bit precision adders and there are only n_l OR gates in the lower significant sub-adder. To produce the carrier signal aimed at the precision adder an additional AND gate is utilized, this LOA architecture is generalized into an architectural template as optimized lower part constant OR adder (LOCA). Approximate least significant bit (LSB) adder (ALA) [5], consist of dual adder sections an precise maximum significant adder section then an LSB approximated with inaccurate adder components. The iterative calculations in intermediary constraints beginning the minimum significant sub-adder constituting the ALA towards maximum significant sub-adder block, calculation period upsurges linearly through the scope of the adder [6]. has submitted an parallel prefix adder, that use majority logic to provide two contributions to the design of the adder. The major involvement is present over a novel characterization of group's common gate equation generation and grouped propagation signal, thereby generating output carry with reduced delay. The second contribution uses the unique recursive attribution in popular logic en route for save circuit complication aimed at use in pre-adders. Generally, the intention present at output carry in n-bit adders results in 40% delay reduction.

For the implementation of full adder circuits hybrid logic style is exploited. The design based on hybrid MTJ/CMOS (Magnetic tunnel junction/Complementary metal–oxide–semiconductor)can solve the leakage problem and bring the advantage of non-volatility using low power magnetic full-adder (MFA) [7]. MFA can withstand any particle impact, regardless of the induced charge, however radiation induced soft errors are still a problem in this adder. Many circuits with hybrid structure have been implemented, which are faster than the C-MOS and ingest less power and this presentation is used in several applications like portable and IOT (Internet Of Things) devices. It is predictable to use simple and effective timing behaviors like conventional logic effort to analyze hybrid adder circuit [8]. In accurate selection, the introduced standards are gain and selection factor and for the administration of energy efficiency and performance adjustment, hybrid adder cells are calculated over single test bench for the period of optimization. In relations of delay, power and driving capability hybrid FA's [9] enactment is mostly hooked on the XOR-XNOR circuit enactment. Cadence virtuoso environs with 90-nm CMOS expertise is used for the recreation of this enactment. The driving capabilities are calculated by 2, 4, 8-bit cascaded full adder with inserted FA's, it minimize the power delay up to 7.5%. For examining state-of the art approximate adders [10] designed on behalf of executing ASIC in add yet shift accelerators to practice the function of video and image. In the existence of frequent and low magnitude sum errors, then the description is done by the approximate adders. This adder provides main concern towards the power-efficiency, and results in the reduction of power about 7.7%. The adders output by means of fault is demonstrated by means of single stuck at fault, and its exists fought through the appraisal with projected similarity in sum using similarity of sum (i.e., sum bits are compared with the carry output) in multi-block carry select adder [11]. In this adder the appeared fault is spotted in advance the existence of next fault, the detection of error and easy testability functions are used to predict the fault all through the process. New full swing XOR-XNOR or XOR/XNOR gates [12] based hybrid 1-bit full adder [13] takes its scheduled qualities as speed, power consumption, power delay product, driving ability etc. This adder overcomes the disadvantages like critical path and positive feedback on output side.

Accuracy-configurable adder (ACA) [14] design is urbanized to accommodate dynamic level of calculation, and delay adaptive self-configurable performance is projected to develop accuracy delay

transaction. Clamped-clamped micro beam resonator based on digital circuit execution through multiple split electrodes, where the resonant frequency is regulated by input logics in compact full adder [15]. Logic inputs resonant frequency is used to operate this adder, in which the input and output of the resonator are not well-matched. Computation in memory parallel adder [16], is used to analyze the feasibility in depth and it contains high scalability. Parallel addition is established by scheduled binary reduction tree yet lower bound time complication ($\log_2(N)$), their equivalent adders are recorded as of right to left on behalf of the optimization area. In BCD (Binary Coded Decimal) adder [17], the carry computation is used on behalf of calculating the total output carriers in multi-digit BCD adder in parallel, BCD carriers are evaluated by decimal group create and broadcast signal, the delay in this adder is minimized about 38%. Behalf of direct or post-truncation full width adder tree (AT) get established, after this fixed-width adder tree is attained (AT) [18]. The huge volume of error is caused at FX-AT output due in the direction of the introduction of truncated input, in which the output is biased nearly and enhances the appeared block. The structure of block-based carry speculative approximate adder [19] is non-overlapped summation block with adder partitioning is obtained by carry propagate yet parallel-prefix [20] adder. Error detection yet recovery mechanism be used to maximize accuracy and minimize output error, where the average reduction is about 50%. Reconfigurable approximate carry look-ahead adder (RAP-CLA) [21], consumes skill to switch in the middle of estimated and precise operating mode that is favor for cross resilient and exact application, state of the art reconfigurable adder is attained through certain alteration in CLA adder. Power ingesting through this adder is of about 19%. Inexact floating point adder is suggested in [22], to perform the operations like normalization and rounding. By this adder high dynamic range images are treated to view the inexact design, the power delay is of about 39.60%. HUB-floating point adder [23] is constructed on dual path procedure, where each path works in parallel to minimize the execution time. In [24], the suggested adder is Tunable Floating Point (TFP) where the specific number of bits for substantial and exponent in the floating point illustration, in which the power efficient is calculated. The pair of circuit is used in the application of ternary half adder [25] with the improvement of multi-level ternary and basic binary circuits in which one path diminishes the computational resource through the power delay of about 63%.

In this paper, we focus on the novel parallel adder that attained from the carry look-ahead adder. Carry look-ahead adder expands speed via minimizing the propagation time in determining carry, and extensively utilized in all electronic circuits and cannot fulfill the expected goal. To overcome this, a novel parallel adder is suggested to recognize efficient enactment. In this proposed system, simulation is prepared for 8-bit input data. The speed and power consumption and power speed products are measured for performance analysis.

2 Proposed XOR-XNOR Cell

2.1 Proposed XOR-XNOR Cell Scheme

In Fig. 1, the module 1 structure represents the XOR-XNOR cell that create a signal H and $\bar{H}$ that initiate inputs for following two modules. To understand this module discrete logic type based topologies have suggested in this literature. New XOR-XNOR high performance circuit is designed at the remainder of this section.

The circuit at Fig. 2 represents the proposed XOR-XNOR cell where, both the outputs are created instantaneously. From the Fig. 2, the weak logic '0' ($|V_{TP}|$) seems at the output H, once both the inputs are fixed at low level. Even so, the pMOS transistor is turned ON with this responsibility in feedback-loop (M_{PF}). After this the nMOS transistor is turned ON via passing the logic '1' in feedback-loop (M_{NF}) and at H output, logic '0' is created intensely. The weak logic '1'($V_{DD} - V_{TN}$) seems by the side of output $\bar{H}$, once both the inputs remain in elevation. As per the case, by way of passing logic '0' by the side of output H, M_{NF} switch is ON then strong logic '1' is delivered by the side of output $\bar{H}$ and M_{PF} is

switched ON. The seamless voltage level is provided by the side of output intended for new combination of inputs. Next two hybrid full adder modules are initiated by the help of these features.

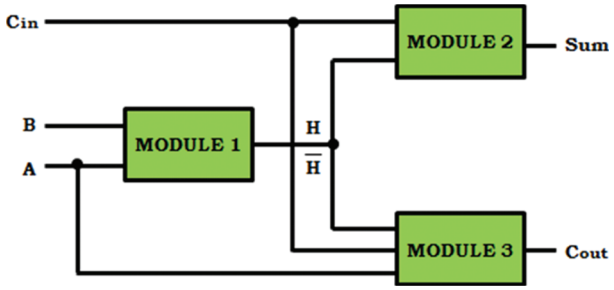

Figure 1: Hybrid design of full adder cells

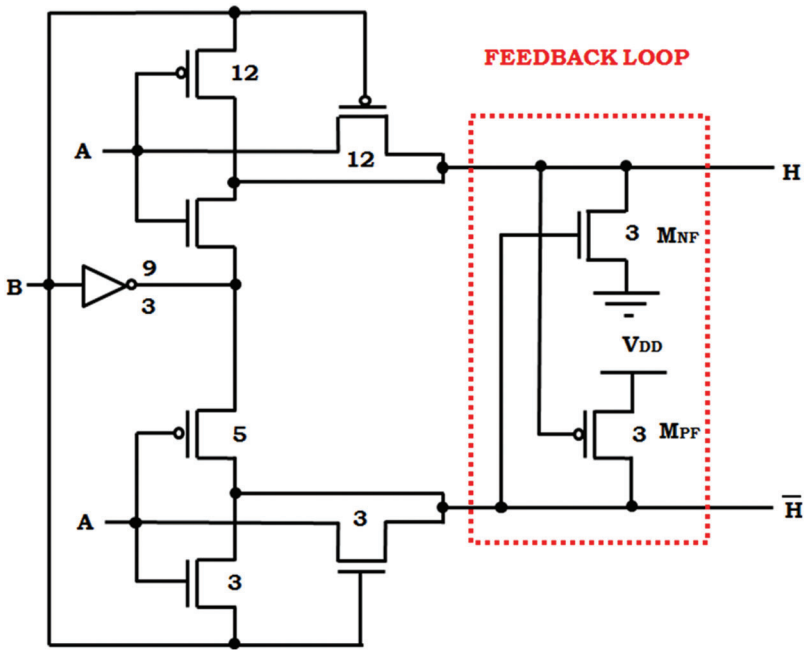

Figure 2: Proposed XOR-XNOR cell

The XOR-XNOR cell consists of 12 possible transitions (Initiated by the combination of input, AB = '00' and it is varied to '01', then again to '00' now it is changed '00' to '10' and rapidly goes on, thus the formation of the 12 transitions are achieved). The time interval of the input to obtain the voltage supply of about 50% and the same level obtained by the output are calculated yet the obtained worst-case is recognized as the cell delay propagation. The average of the power dissipation is fixed from the consumption of average power in all illustrations are considered from the 12 transition inputs. The value of PDP is calculated as,

$$PDP = Worst\ case\ delay \times Average\ power\ consumption \quad (1)$$

2.2 Proposed Full Adder Cell

The module-2 of proposed hybrid full adder indicates XOR cell and is shown in Figs. 3a–3e. The conventional LP-XOR, 3 T-XOR, inverter-based XOR and P-XOR cells utilize a maximum of only four transistors but they fail to produce full swing output and hence they are not suitable for cascaded architectures. In the proposed XOR cell, a GDI based XOR cell which has four transistors and also provides full swing output is employed to implement module-2 setup.

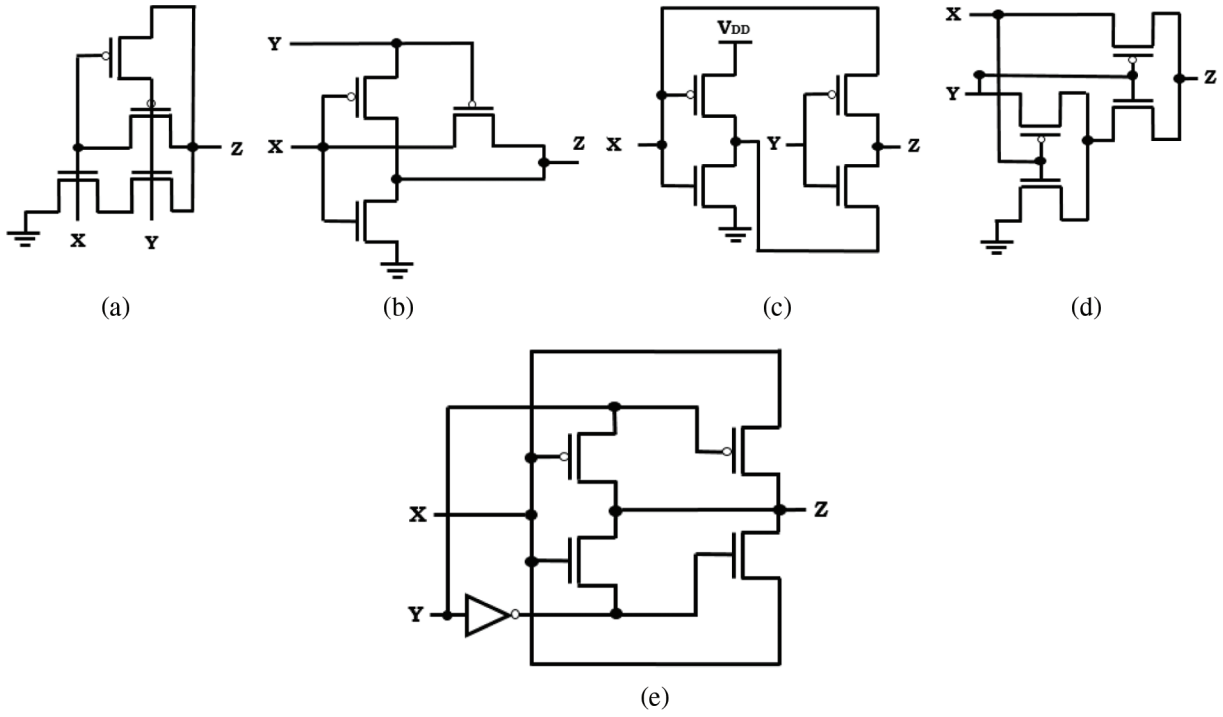

Figure 3: Module-2 circuit possibilities (a) LP-XOR circuit, (b) 3 T-XOR circuit, (c) inverter-based XOR circuits (d) P-XOR circuits

The 2-to-1 multiplexer also remains as hybrid full adder of third module as per the Fig. 1. Certain suggested 2-to-1 MUX circuits are characterized at Fig. 3, in which the input, select lines then outputs be signified as sel, x, y also z correspondingly.

Two pass transistor is used by 2-to-1 multiplexers in Figs. 4a–4c, however the generated output is an non-full swing this is the major dis-advantage. Improper concert is yielded by the entire circuits because of the occurrence of voltage degradation, this happens when the successive stages are connected by the degraded output. This declared tricky is eradicated through concerning two circuits of Fig. 3c composed with Fig. 3d, however the single pMOS and single nMOS transistors are conducted at the respective combination of input. At node z, logic '0' is yielded by way of passing logic '0' over Mn2 when the occurrence is set to sel = x = 0 else the logic '1' is yielded by way of passing logic '1' over Mp2 at the occurrence sel = y = 1. In the design of our full adder, at Fig. 3d, 2–1 MUX is nominated in place of module 3 to gratify the property full-swing.

2.3 Design of Proposed Full Adder Cell

The whole circuit of the suggested hybrid full adder is employed by Fig. 1 configuration is demonstrated in Fig. 4.

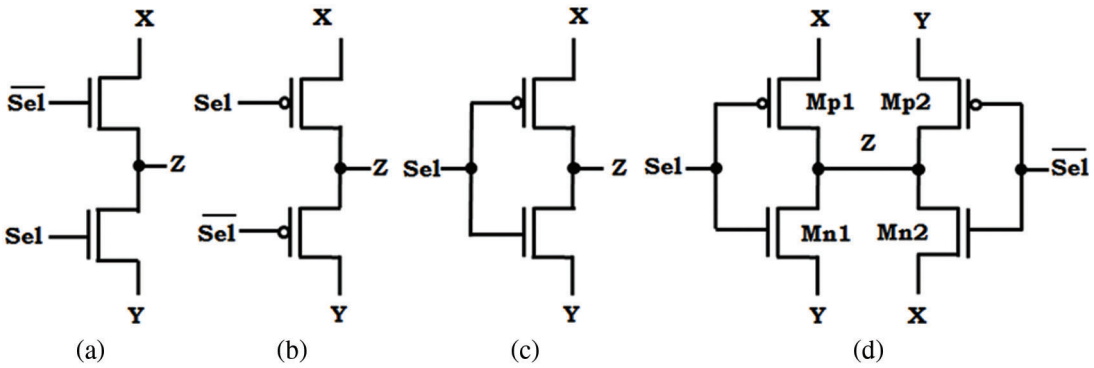

Figure 4: 2:1 Mux circuit topologies

The full-swing property is assured and the outputs are created independently, in this suggested full adder, which is illustrated in Fig. 5. To achieve the target of small chip capacity, the 18 MOSFETs are used totally to design the circuit. The considered XOR-XNOR cell's speed is utilized as Module 1 by the suggested full adder circuit is satisfactory. Only two-pass transistor is used to perform the input carry to output carry propagation in our proposed design, hence reduce of the RCA's cascaded structure's speed is affected by the delay in propagation of carry this is an advantage of our design.

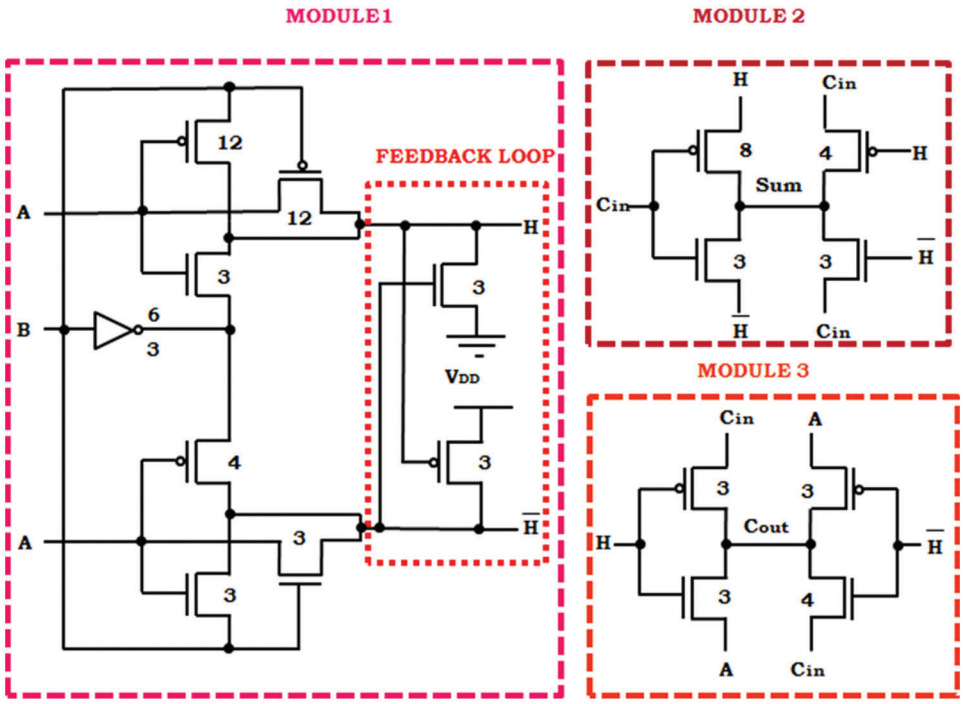

Figure 5: Transistor level proposed full adder

Static and dynamic are the two major constituents of CMOS in the consumption of power (switching and short-circuit are the other two contributes of dynamic power), it is represented as,

$$P_{total} = P_{dynamic} + P_{static} = P_{switching} + P_{short-circuit} + P_{static} \quad (2)$$

$$= V_{DDf} \sum_i V_{i,swing} C_{i,load} \alpha_i + V_{DD} \sum_i I_{i,sc} + V_{DD} I_l \tag{3}$$

Clock frequency, voltage swing at node i, capacitance load at node i, activity factor at node i are represented as f, $V_{i,swing}$, C_i, α_i, $I_{i,sc}$, I_l. $I_{i,sc}$ and I_l are represented for short-circuit yet leakage current. The short-circuit power of the whole adder is minimum and it is obtained through $I_{i,sc}$, VDD and GND are not connected directly in the module 2, 3 circuits and a single inverter is used in our new full adder cell. The hybrid full adder arrangement that used in the suggested system design is used in minimizing the intermediate node and the quantity of 'i' in the switching power component and good layout scheme for the transistor employment.

3 Result and Discussion

The operation of the proposed full adder shown in Fig. 6 is exhibited in the simulation environment. To provide a realistic environment, the buffers are used at the input and output of the cell. The maximum number of transistor used in this proposed adder is 16 with 1.8 V supply voltage and 100 MHz frequency in 180 nm technology. At the output of adder cell, an inverter is connected in series with the load capacitance. The size of buffer and inverter are restricted by signal degradation and fan-out. The entire work is validated in xilinx ISE Desigh Suite 13.4 software.

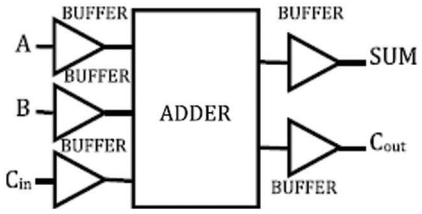

Figure 6: Simulation setup

The layout of proposed 1-bit full adder shown in Fig. 6 is drawn in cadence tool using two lines as per the design procedure. The ultimate aim of designing any VLSI adder is to minimize the circuit area, time delay and power however it is difficult to reduce all factor simultaneously. Hence for effective comparison, the tradeoffs among the factors are needed to be considered. The overall performance of the adder is accessed by measuring the values of FOM. The FOM is expressed as

$$FOM = \frac{1}{power \times Delay \times Area} \tag{4}$$

The full adder performance in contrast to the input noise is assessed by eliminating the input buffers and the input cells are linked straightly towards the full adder cells. The scalability in our proposed adder is best when compared with other adders. The presentation of the suggested full adder is examined in contrast with environmental conditions and variations in manufacturing and this performance are represented in the Fig. 7.

The full adder circuit is designed to moderate the consumption of power values, area and delay these are the major resolution of this adder. Thus these improvements are done by our proposed novel parallel adder. To prove the performance of the proposed adder the comparison is made between several set of adders, which is portrayed in Figs. 8–11. And the comparative analysis of different 1-bit adders is provided as shown in Tab. 1.

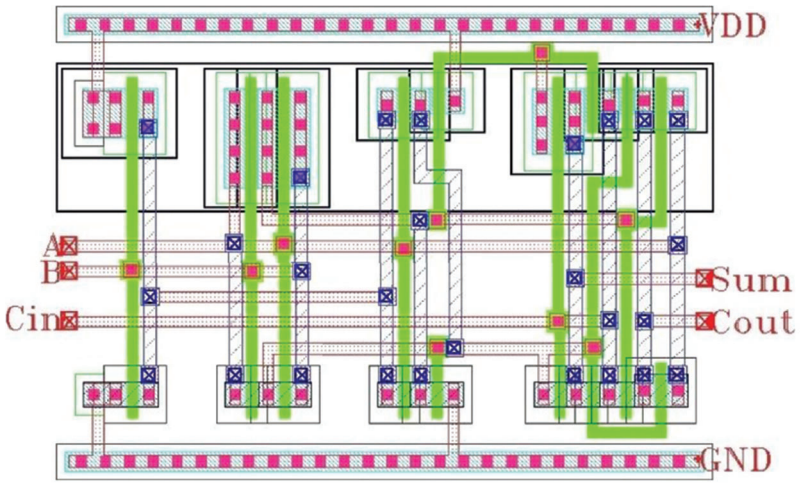

Figure 7: Layout of proposed 1-bit

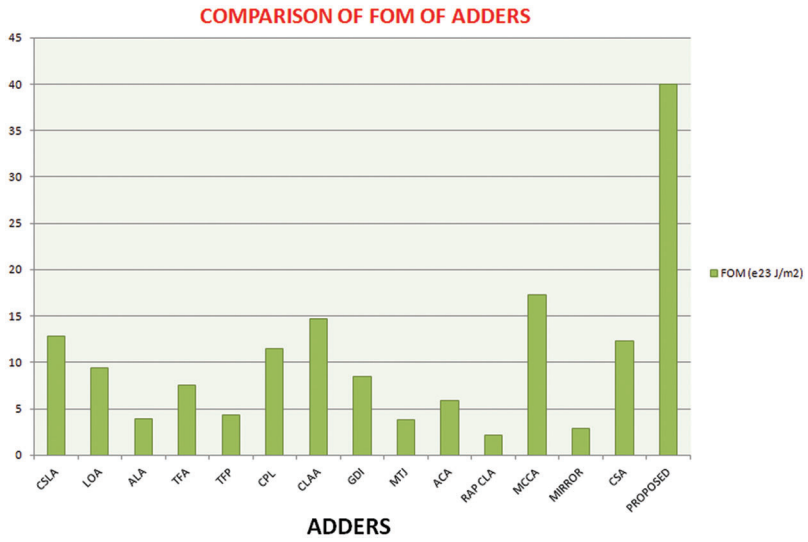

Figure 8: Comparison of FOM of various adders

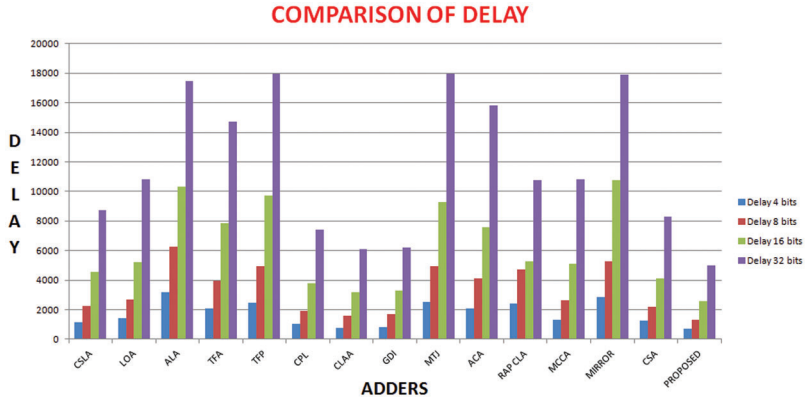

Figure 9: Comparison of delay of 4-bits, 8-bits, 16-bits and 32bits adders

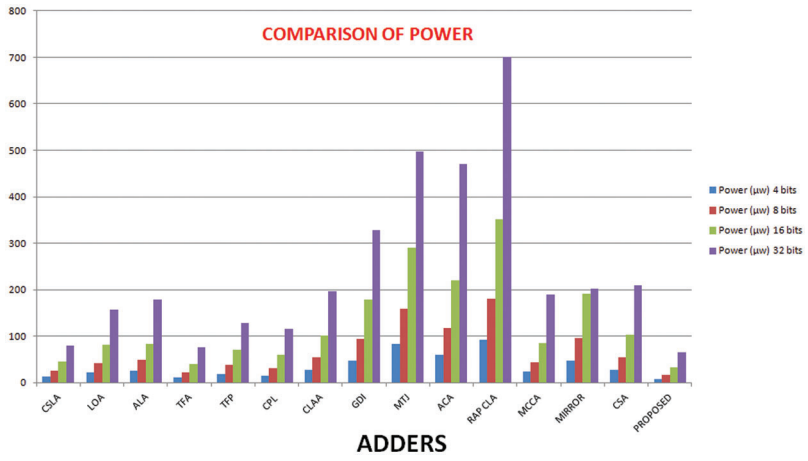

Figure 10: Comparison of power of 4-bits, 8-bits, 16-bits and 32bits adders

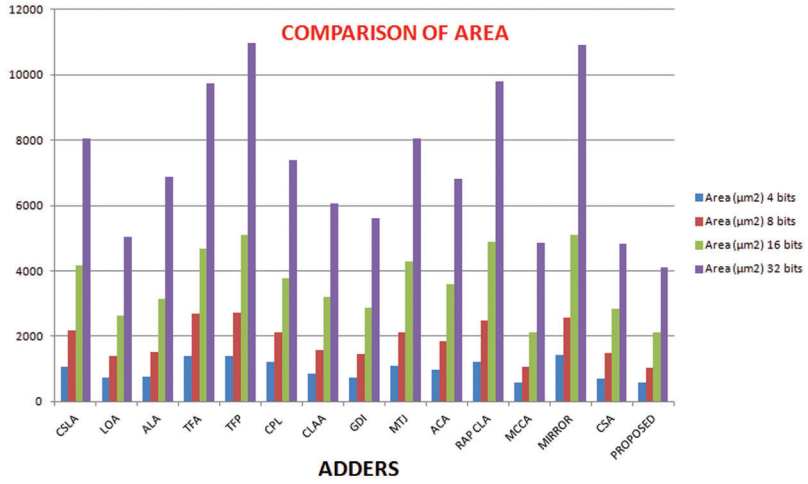

Figure 11: Comparison of area of 4-bits, 8-bits, 16-bits and 32bits adders

Table 1: Performance comparison of various 1-bit full adder

Adder	Number of transistors	Delay (ps)	Power (µw)	Area (μm^2)	PDP (fJ)	FOM (e^{23} J/m^2)
CSLA	24	390	7.85	255.41	3.06	12.79
LOA	20	471	11.94	188.95	5.62	9.41
ALA	22	343	13.65	199.01	4.68	3.90
TFA	20	532	7.24	342.83	3.85	7.57
TFP	16	598	10.45	366.25	6.25	4.37
CPL	28	273	8.23	402.73	2..25	11.5
CLAA	22	212.5	14.61	218.63	3.10	14.73

(Continued)

Table 1 (continued)

Adder	Number of transistors	Delay (ps)	Power (μw)	Area (μm^2)	PDP (fJ)	FOM (e^{23} J/m^2)
GDI	22	230	24.92	205.42	5.73	8.49
MTJ	24	460	15.86	360.33	7.30	3.80
ACA	24	510	11.71	282.48	5.97	5.93
RAP CLA	28	670	17.35	391.47	11.62	2.20
MCCA	16	330	12.15	144.52	4.01	17.25
MIRROR	28	375	24.89	370.26	9.33	2.89
CSA	23	317.5	14.72	173.48	4.67	12.33
PROPOSED	16	212.7	5.97	196.98	1.27	39.98

To get optimized performance from the proposed adder, the power, delay and its product are minimized by reducing the transistors sizes. In an ideal environment, several existing competitive adders are considered to compare with the proposed 1-bit adder. The CPL and RAP CLA adder require 28 transistors whereas the proposed cell requires only 16 transistors. Even though, the MCCA cell has less number of transistors, the delay (330 ps) is comparatively higher the proposed cell. Among the available adders, the power consumption of MIRROR and GDJ are very high while the CSLA, ALA and the proposed cell require less power.

It is necessary to improve the performance of designed 1-bit adder cell so that it will perform well when deployed in real time environment. This is significantly important for cascaded connected adders where the drivers may not give sufficiently strengthened input signal to the cells. The total mortification in signal level may prompt defective yield and the circuit may glitch under low voltages.

The inputs of the adder cells are fed via the buffers to include the consequences of input capacitances and the outputs are also stacked with buffers to ensure proper loadings. The full adder is also experimented in simulation setup. These test benches have three similar buffer prototypes at the input and two at the output. The only difference is the number of adder stages used in between the input and output as well as the number of stages increases gradually depending on number of bits involved. It is noticed that the propagation delay starts to rise significantly in the order of two. The performance parameters (delay, power and area) are measured individually for 4 bits, 8 bits 16 bits and 32 bits as shown in Tabs. 2, 3 and 4. Numerous arbitrary test patterns were given at the inputs and the simulation results of the adder cells were used for comparison. The performance analysis of the proposed full adder was performed with variation in number of bits for 180 nm technology.

While testing, the design with the fewer input, the proposed adder plays a better performance and for some input patterns it stuck with errors. These patterns are delivered as the input towards the design yet the output is noted at the condition for which each required output is corresponding to the each input, thereby the design is set free from the errors. The error stuck that present in the design after manufacturing is found by utilizing these patterns. The input test patterns that essential to investigate a number of adder's 8-bit, 16-bit, 32-bit and 64-bit are shown at the Fig. 7.

Table 2: Comparison of delay of various full adders

Adder	Delay (ps)			
	4 bits	8 bits	16 bits	32 bits
CSLA	1150	2256	4567	8735
LOA	1425	2679	5234	10847
ALA	3186	6257	10314	17462
TFA	2074	3952	7864	14728
TFP	2493	4918	9738	17973
CPL	1042	1948	3783	7398
CLAA	780	1583	3189	6094
GDI	834	1695	3287	6218
MTJ	2519	4958	9283	17936
ACA	2108	4106	7591	15827
RAP CLA	2405	4723	5276	10785
MCCA	1337	2652	5103	10843
MIRROR	2853	5257	10783	17902
CSA	1237	2195	4138	8302
PROPOSED	739	1337	2589	5012

Table 3: Comparison of power of various full adders

Adder	Power (μw)			
	4 bits	8 bits	16 bits	32 bits
CSLA	12.87	25.13	44.72	79.66
LOA	22.63	42.76	81.34	156.32
ALA	25.81	49.64	83.75	178.09
TFA	11.94	21.78	40.32	75.25
TFP	19.27	38.92	70.58	128.72
CPL	15.71	31.63	59.42	115.30
CLAA	27.64	54.56	100.78	197.36
GDI	47.27	94.27	179.56	327.567
MTJ	83.24	158.28	289.43	497.21
ACA	60.14	118.34	220.89	470.24
RAP CLA	92.61	180.37	350.67	700.78
MCCA	23.97	43.89	85.12	189.243
MIRROR	47.26	95.37	191.86	201.53
CSA	27.95	55.18	103.63	208.55
PROPOSED	8.52	16.74	32.76	65.08

Table 4: Comparison of area of various full adders

Adder	Area (μm^2)			
	4 bits	8 bits	16 bits	32 bits
CSLA	1053.76	2186.51	4166.27	8035.12
LOA	721.49	1398.33	2634.78	5047.66
ALA	761.28	1514.69	3143.22	6862.99
TFA	1392.32	2698.62	4687.20	9728.44
TFP	1403.55	2706.28	5109.23	10973.38
CPL	1208.24	2109.98	3783.66	7398.36
CLAA	853.82	1581.54	3189.32	6049.92
GDI	732.77	1466.37	2873.98	5618.25
MTJ	1084.76	2107.28	4283.09	8036.96
ACA	967.61	1845.42	3591.77	6827.57
RAP CLA	1208.48	2479.74	4876.11	9785.79
MCCA	568.32	1052.65	2103.88	4843.44
MIRROR	1409.37	2578.16	5083.17	10902.05
CSA	708.94	1495.83	2838.14	4836.22
PROPOSED	578.58	1037.22	2109.04	4101.62

4 Conclusion

In this paper, the markedly improved novel hybrid adder is presented and implemented with different logic styles. The attributes of proposed adder are compared with various digital adders to prove the effectiveness of proposed scheme. Initially XOR-XNOR cell is modeled then with the help of this cell, a novel parallel adder is designed by incorporating additional modules. When extended for higher bits, the strength of this adder is improved by eliminating the buffers at the input and output ports. This proposed adder is then compared with various adders that are proposed in the previous and obtain the power consumption of about 18% when compared to other adders it is less. The proposed novel parallel adder is designed to dissipate low power, consume less area and operate at high speed. From the comprehensive comparative analysis, it is clear that a high scalability and FOM was delivered by the designed adder cell even when the bit length has been extended up to 32bits. Further the performance of proposed adder with cascaded configuration is to discussed in future.

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