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Process Tolerant and Power Efficient SRAM Cell for Internet of Things Applications

T. G. Sargunam[1,2,*], Lim Way Soong[1], C. M. R. Prabhu[1] and Ajay Kumar Singh[3]

[1]Faculty of Engineering and Technology, Multimedia University, Melaka, 75450, Malaysia
[2]School of Engineering and Computing, Manipal International University, Nilai, 71800, Malaysia
[3]Electronics and Communication Engineering Department, NIIT University, Neemarana, 301705, India
*Corresponding Author: T. G. Sargunam. Email: sargunam.thirugnanam@miu.edu.my
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Abstract: The use of Internet of Things (IoT) applications become dominant in many systems. Its on-chip data processing and computations are also increasing consistently. The battery enabled and low leakage memory system at subthreshold regime is a critical requirement for these IoT applications. The cache memory designed on Static Random-Access Memory (SRAM) cell with features such as low power, high speed, and process tolerance are highly important for the IoT memory system. Therefore, a process tolerant SRAM cell with low power, improved delay and better stability is presented in this research paper. The proposed cell comprises 11 transistors designed with symmetric approach for write operations and single ended circuit for read operations that exhibits an average dynamic power saving of 43.55% and 47.75% for write and 35.59% and 36.56% for read operations compared to 6 T and 8 T SRAM cells. The cell shows an improved write delay of 26.46% and 37.16% over 6 T and 8 T and read delay is lowered by 50.64% and 72.90% against 6 T and 10 T cells. The symmetric design used in core latch to improve the write noise margin (WNM) by 17.78% and 6.67% whereas the single ended separate read circuit improves the Read Static Noise Margin (RSNM) by 1.88x and 0.33x compared to 6 T and 8 T cells. The read power delay product and write power delay product are lower by 1.94x, 1.39x and 0.17x, 2.02x than 6 T and 8 T cells respectively. The lower variability from 5000 samples validates the robustness of the proposed cell. The simulations are carried out in Cadence virtuoso simulator tool with Generic Process Design Kit (GPDK) 45 nm technology file in this work.

Keywords: SRAM cell; low power; process efficient; read stability; write ability; static noise margin; PVT variation; internet of things

1 Introduction

The Internet of Things (IoT) applications are becoming part and parcel of our daily life. IoT applications are used in almost all the industry verticals ranging from manufacturing, healthcare,

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tourism, agriculture, transportation, tele-communication to many others. The IoT revolution does not leave any industry behind. There is a tremendous growth and a huge demand for the IoT based systems. Some of the example applications are smart cities, smart buildings, smart homes, smart agriculture and smart systems. The technologists confirm that IoT and its applications will be driving the human sensations in the future [1]. The IoT application connects a multiple number of portable and battery-operated gadgets by using a wireless sensor network (WSN). The most critical requirements for these IoT application devices are smaller chip area and lesser power consumption [2]. The WSN performs a vital role in these applications. Basically, it offers the communication and connectivity to gather data between the nodes and the base-station for further processing. The nodes communicate with the base-station using wireless protocols [3]. The memory has become the major portion of these modern architectures. The design of static random-access memory (SRAM) is becoming highly critical for any trending application and is one of the most common memory architectures due to its performance [4].

The IoT based low power applications demand the cache memory designed with SRAM due to its high performance and low power features. There are many proposed design techniques for low power and energy efficient SRAM cell with its merits and demerits [5,6]. It is well discussed in the literature that memory cell normally consumes larger power from the overall power of the system. In low power IoT based system-on-chip (SoC) applications, 40–50% average dynamic power is constantly consumed by SRAM memory [7,8]. The conventional cells such as 6 T and 8 T are proven that they are not suitable for any low power applications. The main generic challenges of these SRAM memory are high power consumption, degraded stability, leakage current, short channel effects (SCEs). Over the years, many researchers have suggested and developed many different approaches and techniques to lower the overall power of cache memory [9,10] e.g., differential operation, loop cutting, staff effect, decoupled read circuit, power gating, single bit line operation, lower the supply voltage and schmitt trigger approach [11–15]. The SRAM cells with separate write and read circuits improve significant stability [16,17]. Although there are many different techniques used to design SRAM cells, the conventional cells are not so suitable for the current and trending IoT applications [18,19] due to its low power requirements. Although, the common challenges may be overcome by these SRAM design techniques, the variation of process, voltage, and temperature (PVT) is normally added up to these challenges. A power efficient SRAM cell is critically required to address the above challenges and to exhibit immunity to process variation with operational reliability. Hence, a process tolerant and power efficient SRAM cell is proposed and designed with the following salient features and novelties in this work:

- The latch circuit is totally disconnected so then the data switches quickly on the nodes during the write operations which results the dynamic power consumption less due to lesser discharging at the bit-lines (BL and NBL).
- There are two signals used which play an important role instead of word-line (WL) for the write operations to enhance the write ability.
- The single ended and separate read circuit reduces the read power, improves the read stability and overall read performance.
- The three N-channel metal oxide semiconductor (NMOS) transistors connected in series of the read circuit reduces the static power and leakage current due to the stack effect.

The rest of the paper is organized as follows: The Section 2 highlights the related works in terms of the comparative SRAM cells. Section 3 presents the detailed design of proposed cell structure as well as the working principles. Further, Section 4 incorporates the various analyses, observations, and results outcome of the proposed 11 T cell and comparative cells 6 T [20], 8 T [21], 10 T [22], and 11 T [23] with respect to power consumption, delay, energy efficiency, stability, area, and PVT variations. Section 5 discuss the Monte-Carlo simulation results and statistical variability. Finally, the Section 6 concludes the paper.

2 Related Works

The conventional cells such as 6 T cell and 8 T cell are industry standard architectures which normally used as the reference to benchmark the SRAM performance. The researchers have proposed many budding SRAM cell topologies with enhanced outcome while comparing with these traditional topologies [11–15]. However, in common these cells suffer from conflict between read and operations, degraded stability, half select issue, write failures etc. Further, if the read static noise margin is improved, then it may affect the write operation. The researchers have also forecasted that the process variation may limit the required minimum voltage for the write and read operations. There have been so many improved SRAM cells proposed by researchers [11–15] to enhance the outcomes against conventional 6 T cell.

In this research, the conventional 6 T [20], standard 8 T [21], low power and high speed 10 T [22] and multi-bit error tolerant 11 T [23] have been chosen for review and for benchmarking. These cells are redesigned at schematic and layout in same environment and then compared against the proposed cell. All these cells' schematic representation is shown in Figs. 1 and 2. The operational specifications of the selected cells are highlighted in Tab. 1. The comprehensive process variation analysis of the proposed cell and the selected cells are discussed in detail in this paper. Despite having so many different cells with various techniques, the research is still open for SRAM cell design in terms of minimizing power, improving performance, better write ability and read stability, less leakage current, energy efficient and process tolerance for IoT applications.

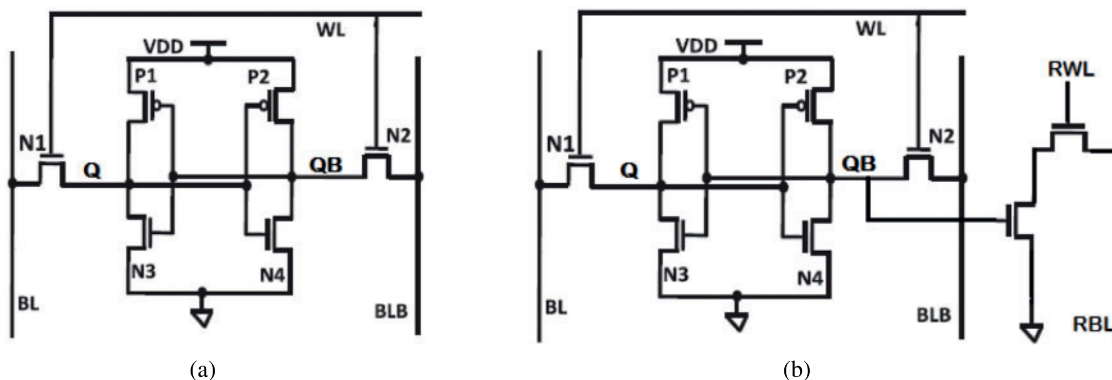


Figure 1: SRAM structure: (a) 6 T SRAM cell [20] (b) 8 T SRAM cell [21]

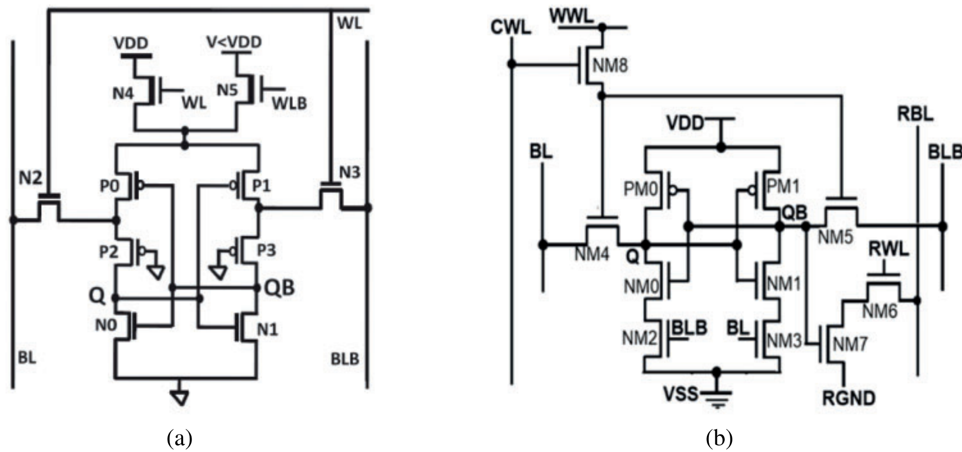


Figure 2: SRAM structure: (a) 10 T SRAM cell [22] (b) 11 T SRAM cell [23]

Table 1: Operational specification of all the cells

Cell Feature	6 T [20]	8 T [21]	10 T [22]	11 T [23]	11 T (proposed)
Write operation	Differential	Differential	Differential	Differential	Differential
Read operation	Differential	Single end	Differential	Single end	Single end
Bit-lines	2-BL/BLB	3-BL/BLB/ RBL	2-BL/BLB	3-BL/BLB/ RBL	3-BL/NBL/ RBL
Control signals	1-WL	2-WL/RWL	2-WL/WLB	4-WWL/CWL/ RWL/RGND	4-WL/RWL/ LW/RW
No. of NMOS Transistors in Read path	-	2	-	2	3

Notes: WL: Word line; RWL: Read word line; RBL: Read bit line; WWL: Write word line; CWL: Column word line; RGND: Read ground; BL, BLB, NBL: Bit lines.

All the selected SRAM cells perform the write and read operations on differential mode except 8 T [21] and 11 T [23] cell work on single end read operation. The number of bit-lines are 2 to 3 in all the cells. The common control signals are WL for write and RWL for read operations. The number of transistors used for single end read operation is 2 and 3 for 8 T [21] and 11 T [23] cells. Summarizing all the highlighted challenges, a power efficient and process tolerant 11 T SRAM cell is proposed in this paper. Besides the comprehensive analysis of proposed 11 T cell, several comparative analyses are also carried out and compared with selected conventional 6 T [20], standard 8 T [21] and low power and high speed 10 T [22] and multi-bit error tolerant 11 T [23] cells.

3 Proposed Process Tolerant and Power Efficient SRAM Cell

3.1 The Cell Structure

The schematic architecture of the proposed cell is shown in Fig. 3. The proposed cell consists of 11 transistors (11 T) with separate write and read circuits to minimize the power and enhance the read

static noise margin without any compromise on delay. The proposed cell has two inverters on both sides. The left side inverter is composed by transistors PM1, P-channel metal oxide semiconductor (PMOS) and NM1, N-channel metal oxide semiconductor (NMOS) and right one by PM2 and NM2. The NM3 and NM4 tail transistors play a vital role during the write operations. They pull either logic high or low at output nodes which improves the cell's write ability. The signals LW and RW control the switching activity of these two tail transistors. The inverter performs write operation quicker without waiting for the bit-line to discharge and hence it saves reasonable dynamic power. The BL and NBL bit-lines are connected to Q and NQ output nodes through the NMOS transistors NA1 and NA2. These two transistors (NA1 and NA2) function as access transistors. The write mode operation is jointly performed by the word-line WL and the LW and RW signals in this proposed cell. For the write operation, upon asserting the word-line WL to high, the access transistors NA1 and NA2 are turned ON and the LW and RW signals are alternatively switched ON so that the corresponding data in bit lines can be transferred faster to Q and NQ nodes respectively.

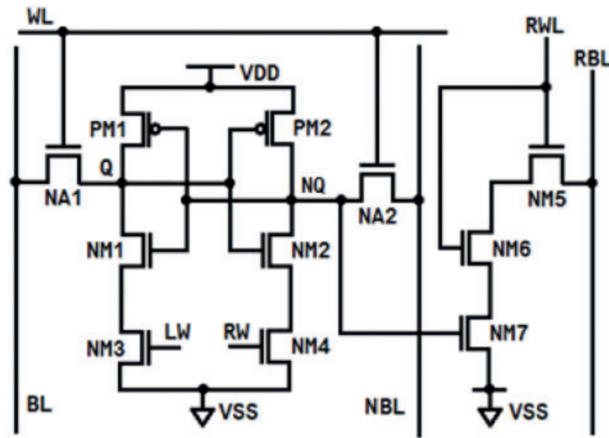


Figure 3: Schematic diagram of proposed 11 T Cell

The single end read circuit is designed with three NMOS transistors NM5, NM6 and NM7 to improve the cell's read stability. The NM5 and NM6 transistors behave as read pass-transistors which controls the read word-line (RWL). The output NQ is connected to the gate of NM7 transistor. During the read mode and hold mode operations, the LW and RW signals are assigned to be high and low as the read operation is done independently. The output nodes are separated from the bit-lines during read and hold mode operations through which the proposed cell's static noise margin (SNM) has been significantly improved. The use of three transistors is to have stack effect which helps to reduce the leakage current in hold mode. The current flow is also limited from read bit-line to ground and hence the power dissipation is less. The status of control signals for write, read and hold state is presented in Tab. 2.

Table 2: Operational table of proposed 11 T SRAM cell

Type	Signal	Write operation	Read operation	Hold state
Control Signals	WL	1	0	0

(Continued)

Table 2: Continued

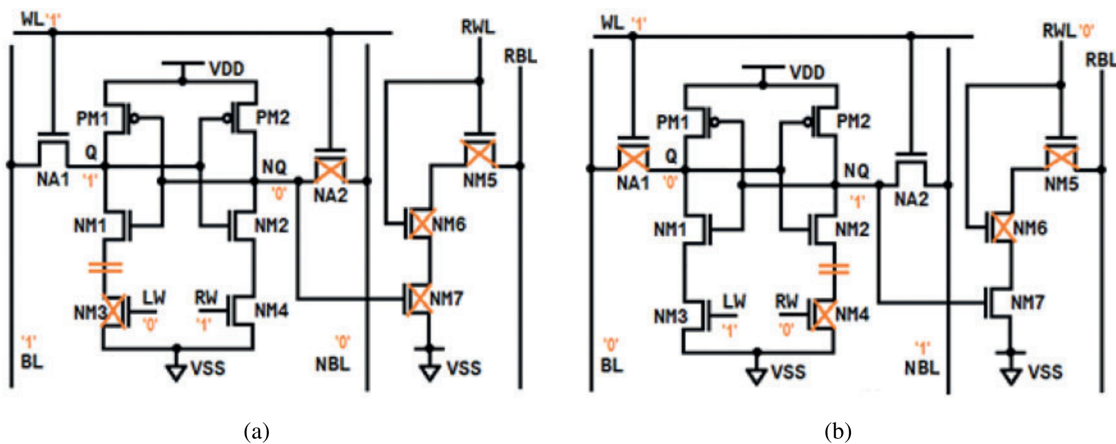
Type	Signal	Write operation	Read operation	Hold state
	RWL	0	1	0
	LW	1/0	1	1
	RW	0/1	0	0
Bit-lines	BL	1/0	precharge	precharge
	BLB	0/1	precharge	precharge
	RBL	0	precharge	precharge

3.2 *Working Principle of the Proposed Cell*

The proposed 11 T cell is designed and implemented in 45 nm complementary metal oxide semiconductor (CMOS) technology. A uniform device size has been applied to PMOS and NMOS transistors for reasonable comparison. The 150 nm/45 nm size has been used for all the PMOS transistors and 120 nm/45 nm is applied for all the NMOS transistors. This combination of device sizing provides the nominal voltage transfer characteristics (VTC). The 1 V supply voltage at 27°C temperature is applied for all the operations.

3.2.1 Write Operation

The transistors NA1 and NA2 flip the data quickly at the storage nodes due to the proposed cell's dynamic nature. During the write operation, the word-line WL is asserted to high and read word-line RWL and PC (to precharge RBL) are set to low after the data is assigned on bit-lines BL and NBL. The LW and RW signals play a significant role instead of WL for the write operations to enhance the write ability. The write circuit of the proposed 11 T cell is shown in Fig. 4. The proposed cell signaling scheme and the status of bit lines and control signals of write operation is plotted in Fig. 6.



(a) (b)

Figure 4: Write mode: (a) Write '1' operation (b) Write '0' operation

For write ‘1’ operation, the bit-line BL is set to high, NBL is set to low and WL is asserted to high. Prior to asserting WL, the LW is set to low and RW signal is high so that NM3 or NM4 transistor is either disconnected or connected from the ground. Once the NA1 and NA2 transistors are turned ON, the respective data in bit-line BL is transferred to Q. When bit-line NBL is assigned to ‘0’, the transistor NM3 turns off due to LW is kept at low. This will disconnect pull down path of left inverter. Hence, the output Q is quickly flipped to high before NBL discharges completely without any waiting.

For write ‘0’ operation, the bit-line NBL is set to high and BL to low. Prior to asserting the WL, the LW is assigned to high and RW signal to low so that NM3 or NM4 transistor is either connected or disconnected from the ground and which causes the data to be stored in NQ. When BL is assigned to ‘0’, the transistor NM4 turns off due to RW is also set to ‘0’ and disconnects pull down path of right inverter which flip the node NQ to high quickly without any waiting for bit-line (BL) to completely discharge. The effect of disconnecting the pull-down path causes low power consumption and improved write access time.

3.2.2 Read Operation

For read operation, the WL is not used and hence set to low. Both bit-lines BL, NBL must be precharged during read operation and RWL is connected to V_{DD}. The separate read circuit would perform either read ‘0’ or read ‘1’ operation which depends on the output data in node NQ. When NQ holds data ‘0’, the transistors in the read path (NM5 and NM6) are turned ON whereas NM7 is turned OFF which will disconnect RBL from ground. The read path is open now and does not allow RBL to discharge. Therefore, RBL holds the pre-charged voltage level which is treated as read 1 operation. If NQ holds data ‘1’, all three transistors (NM5, NM6 and NM7) in read path will turn ON which allows the RBL to discharge fully and sense amplifier will interpret this voltage fall on RBL as read 0. The read circuit is shown in Fig. 5. The proposed cell signaling scheme and the status of bit lines and control signals during read operation is plotted in Fig. 6.

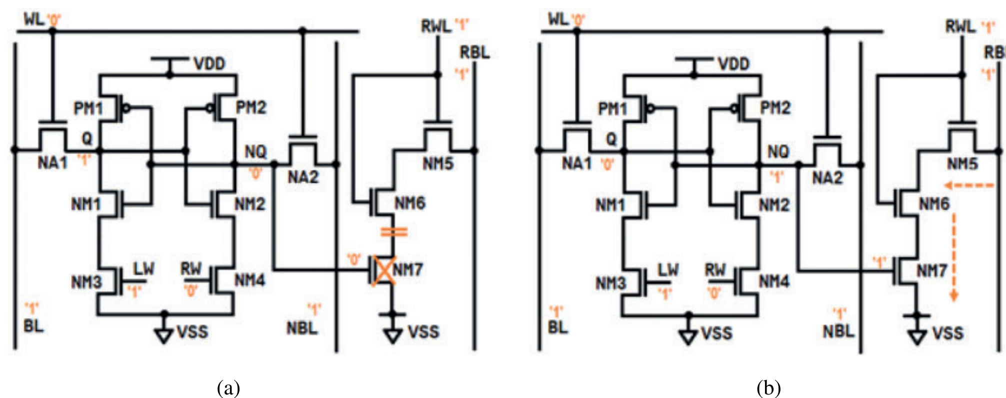
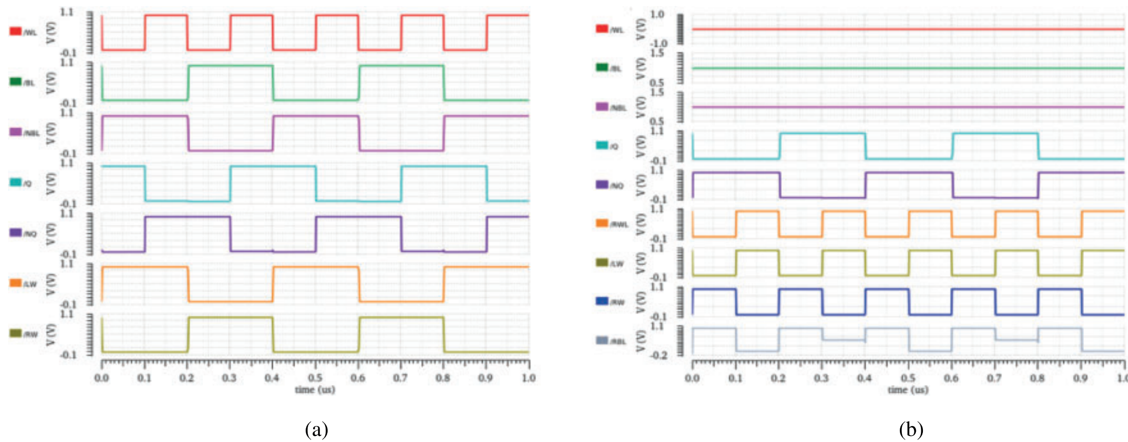


Figure 5: Read mode: (a) Read ‘1’ Operation (b) Read ‘0’ Operation



(a) (b)

Figure 6: Waveform of the proposed 11 T cell (a) Write operation (b) Read operation

3.2.3 Hold Operation

In the hold mode, the access transistors NA1 and NA2 are disconnected from the bit-lines BL and NBL by setting WL to low. The RWL is also set to ground and bit-lines BL and NBL are precharged to V_{DD}. Therefore, the cell is in standby or hold mode. The cell will continue to hold the previous voltage level.

4 Simulation Results and Discussion

4.1 Simulation Setup

The Cadence virtuoso simulator tool using Generic Process Design Kit (GPDK) for 45 nm technology is used to carry out all the simulations in this research work. The respective cells are designed and simulated at 1-V supply voltage and at 27°C temperature. An equal device size is applied for all PMOS and all NMOS transistors for fair comparison [24]. The dynamic power, stability and energy efficiency have been analyzed to determine the cell performance. The PVT variation analysis is also performed for process corners, for temperature ranging from −50°C to 150°C and voltage (V_{DD}) from 200 mV to 1.0 V. The Monte-Carlo (MC) simulation is performed with 5000 samples to investigate the impact of process variations of the proposed cell. The 10% variation of Gaussian distribution with 3σ is assumed in MC analysis.

4.2 Power Dissipation

Power dissipation of SRAM cell is the main constraint with the demand for many simultaneous applications and its operational speed. The system performance and reliability are affected by the power consumption [25,26]. SRAM memory in general consumes 80% of the power from the overall system. The total power dissipation can be in terms of dynamic and static. The dynamic power is consumed during switching, charging/discharging of capacitor. The static power is normally measured during hold mode.

4.2.1 Dynamic Power

The power dissipation is generally more in 6 T, 8 T cells due to discharging activity at both bit lines. The proposed cell consumes less power because of lower discharging activity at respective output

storage nodes. The write and read power of the proposed cell is measured at transient time of 1 μs which is presented in Tab. 3. It is observed from the table that write power of the proposed 11 T cell is 43.03%, and 47.25% lower than the 6 T and 8 T cells respectively. The read power is minimized by 31.12%, 31.42% and 17.76% compared to 6 T, 8 T and 11 T cells.

Table 3: Write/Read power of the proposed 11 T cell

SRAM cell	Write power (nW)	% Difference	Read power (nW)	% Difference
6 T [20]	32.0043	43.03%	70.7157	31.12%
8 T [21]	34.5653	47.75%	71.0227	31.42%
10 T [22]	8.8557	−51.43%	13.2101	−72.88%
11 T [23]	14.5061	−20.44%	59.2244	17.76%
11 T (proposed)	18.2340	-	48.7065	-

The overall dynamic power consumption of the presented cell and other cells from the literature have been measured during the write and read operations for different frequency range (from 5 to 1 MHz) as plotted in Fig. 7. The proposed 11 T cell consumes an average of 43.55%, 47.75% lower power during write operation compared 6 T and 8 T cells on different frequency with less discharging at output nodes. Similarly, the average read power is also lower by 35.59%, 3.56% and 23.98% over 6 T, 8 T and 11 T cells due to a separate read circuit.

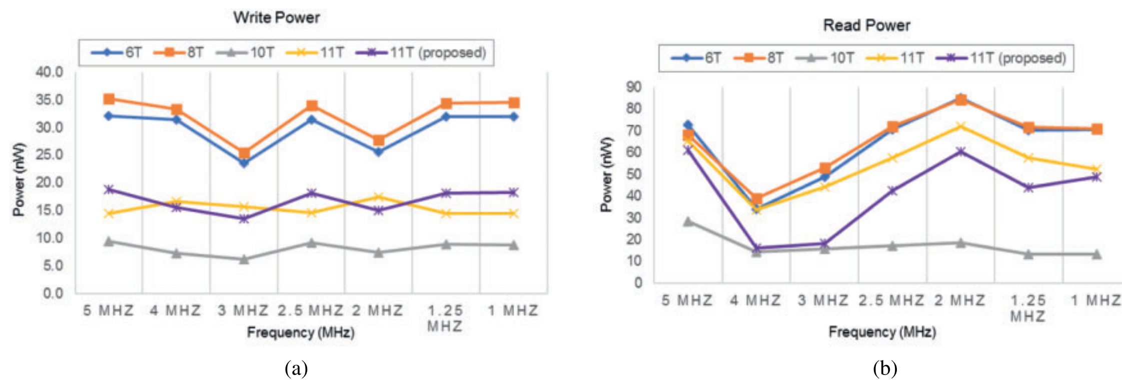


Figure 7: Power of various cells *vs.* frequency (a) Write operation (b) Read operation

4.2.2 Static Power

The static power is measured during the hold mode when there is no activity. SRAM memory's static power is a challenge in the idle state due to tremendous increase in leakage current at transition point. It is generally measured when word-line WL and read word-line RWL are at low. The static power of proposed cell is 42.94%, 43.83% and 30.51% lower than 6 T, 8 T and 11 T cells as shown in Tab. 4. The static power is reduced by the stacking effect induced by the tail transistors NM3 and NM4. The power from the memory during the hold mode is defined as the leakage power which has become a major challenge for cache memory on SRAM cells especially in the nano-meter regime.

Table 4: Static power of the proposed 11 T cell

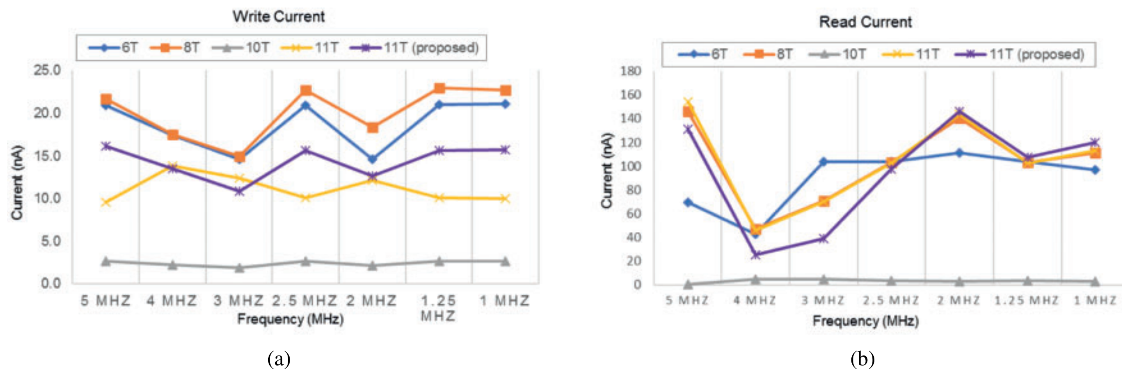
SRAM cell	Static power (nW)	% Difference
6 T [20]	70.4404	42.94%
8 T [21]	70.2984	43.83%
10 T [22]	4.0737	−89.86%
11 T [23]	57.8335	30.51%
11 T (proposed)	40.1900	-

4.2.3 Cell Current

Another important SRAM design parameter is the current. The write/read current of 11 T cell are investigated and measured at transient time of 1 μs which is presented in Tab. 5. The write current of suggested 11 T cell is less than 6 T and 8 T cells. However, the read current of the 11 T cell is 19.17%, 7.15% and 6.04% more compared to 6 T, 8 T and 11 T cells. The overall current of the 11 T cell and other comparative cells from the literature have been measured during write and read operations for different frequency ranging from 5 to 1 MHz and analyzed. The proposed 11 T cell's average current is 83.29% and 22.01% higher than the 10 T and 11 T cells. The average read current is higher than 6 T cell only. The cell current for write and read mode is plotted in Fig. 8.

Table 5: Write/Read current of the proposed 11 T cell

SRAM cell	Write current (nA)	% Difference	Read current (nA)	% Difference
6 T [20]	21.0656	25.19%	97.0769	−19.17%
8 T [21]	22.7555	30.74%	111.5110	−7.15%
10 T [22]	2.6254	−83.34%	2.8685	−97.61%
11 T [23]	10.0197	−36.42%	112.8450	−6.04%
11 T (proposed)	15.7602	-	120.1040	-



(a) (b)

Figure 8: Cell current of various cells *vs.* frequency (a) Write operation (b) Read operation

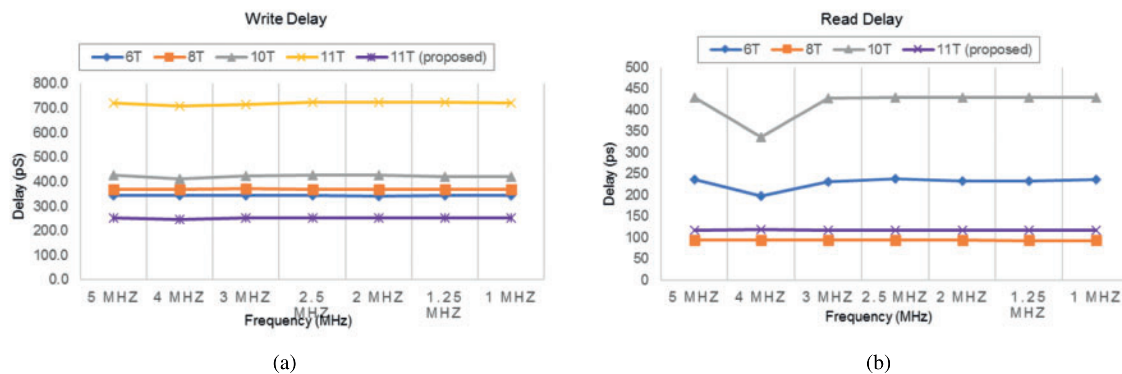
4.3 Delay Time

4.3.1 Write Delay and Read Delay

The delay or access time is normally used to calculate the speed and performance of the SRAM cell. The write delay is measured between the word line WL and either one output Q or NQ from the first rising or falling edge with 50% threshold voltage. The read delay is measured between the RWL and RBL from the first rising or falling edge with 50% threshold voltage. The delay measured at transient time of 1 µs is presented in Tab. 6. The write delay has improved about 26.46%, 37.16%, 40.19% and 65.02% compared to 6 T, 8 T, 10 T and 11 T cells. It is noted from the results that read delay for 11 T cell is high and recorded as 100.908 ns. The read delay is lowered by 50.64% and 72.90% over 6 T and 10 T cells. The delay time has also been measured at various frequency and shown in Fig. 9.

Table 6: Write/Read delay of the proposed 11 T cell

SRAM cell	Write delay (pS)	% Difference	Read delay (pS)	% Difference
6 T [20]	343.658	26.46%	236.095	50.64%
8 T [21]	402.153	37.16%	93.655	−19.64%
10 T [22]	422.555	40.19%	430.049	72.90%
11 T [23]	722.505	65.02%	100.908 ns	-
11 T (proposed)	252.733	-	116.539	-



(a) (b)

Figure 9: Delay of various cells *vs.* frequency (a) Write delay (b) Read delay

4.4 Power Delay Product (PDP)

The energy efficiency of SRAM cell is determined by calculating power delay product (PDP) [27]. The product value of delay and the respective power dissipated for write and read operations are known as power delay product. The cell's potential enhancement is also estimated through PDP calculation for both write and read operations. The Write power delay product (WPDP) and Read power delay product (RPDP) are presented in the Tab. 7. It is derived from the results that proposed 11 T cell's write power delay product is lower by 1.39x, 2.02x, 1.27x over 6 T, 8 T, 11 T cells and read power delay product is 1.94x, 0.17x less against 6 T, 8 T cells at 1 V. In general, the delay (time) plays a major role in the PDP calculation. Moreover, the suggested 11 T cell has the lowest write delay which shows the

significant reduction of energy consumption. The less power delay product confirms that the proposed cell is energy efficient compared to other cells. Even though 8 T cell with least read delay, yet it is noted higher RPDP due to higher power for read operation.

Table 7: Power delay product of various cells

SRAM cell	WPDP (aJ)	Variation	RPDP (aJ)	Variation
6 T [20]	10.999	1.39x	16.696	1.94x
8 T [21]	13.901	2.02x	6.652	0.17x
10 T [22]	3.742	-	5.681	-
11 T [23]	10.481	1.27x	-	-
11 T (proposed)	4.608	-	5.676	-

4.5 Stability

The stability of suggested and comparative cells has been analyzed in terms of static noise margin (SNM). The minimum DC noise that is needed to switch the stored bit in a node is known as SNM. The SNM is normally measured during hold, read and write operations which are named as Hold static noise margin (HSNM), Read static noise margin (RSNM) and Write noise margin (WNM). It is noted that the SRAM cell robustness can be achieved with higher SNM value for all the operations [28]. The traditional butterfly curve technique is used to calculate the static noise margin in this paper [29].

4.5.1 Hold SNM (HSNM)

The HSNM can be defined as the maximum DC voltage that a cell can tolerate without losing data during hold mode. HSNM is measured when bit-lines BL and NBL are connected to V_{DD} (1 V), WL and RWL are connected to the ground (0 V). The HSNM for suggested 11 T, 6 T and 8 T and cells are plotted in Fig. 10. The HSNM of the proposed cell is 400 mV which is nearly equal to other cells.

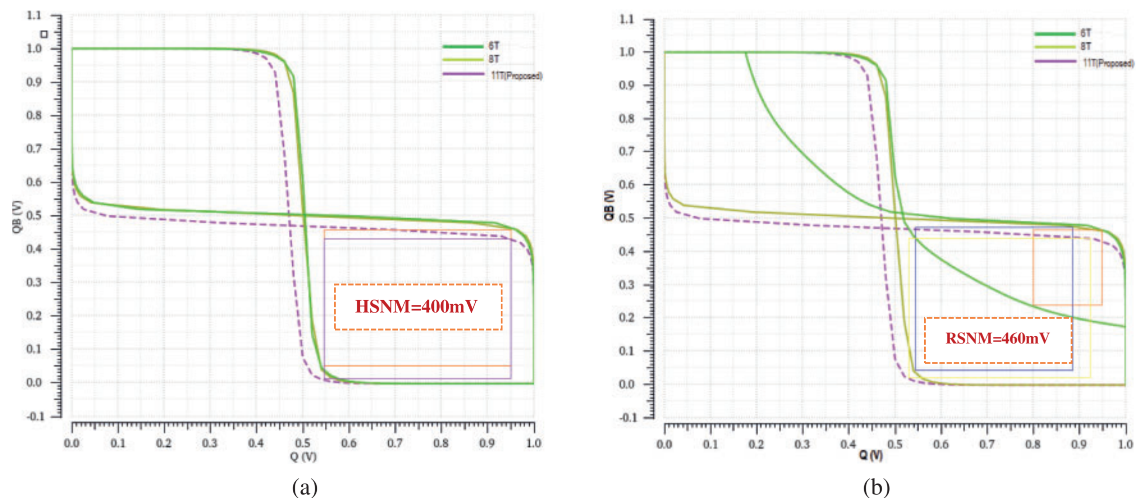


Figure 10: (a) HSNM of 6 T, 8 T and proposed 11 T cells (b) RSNM of 6 T, 8 T and proposed 11 T cells

4.5.2 Read SNM (RSNM)

The read static noise margin is the maximum DC voltage that a cell can tolerate without losing the data in read operation. The RSNM is measured at 1 V supply voltage when bit-lines BL and NBL are connected to V_{DD} (1 V), word-line WL is connected to ground (0 V), RWL are connected to the V_{DD} (1 V) and with RBL precharged. The single ended read circuit with series connected transistors NM5, NM6 and NM7 do not affect the output nodes Q and NQ which results in achieving higher RSNM. The RSNM for 11 T, 6 T and 8 T cells are depicted in Fig. 10. It is calculated that the RSNM of 11 T cell is 460 mV, 8 T is 345 mV and 6 T is 160 mV. It is also evident from the butterfly curve that RSNM of proposed cell is higher and 1.88x and 0.33x improved when compared to 6 T and 8 T cells. The suggested 11 T cell achieves improved read stability.

4.5.3 Write NM (WNM)

The write ability of SRAM cell is measured using write noise margin [30,31]. The WNM is calculated at 1 V supply voltage when bit-lines BL and NBL are assigned with 1 and 0 alternatively for write 1 and 0 operations with WL is connected to V_{DD} (1 V) and read word-line RWL is connected to the ground (0 V). The WNM of 6 T, 8 T and proposed 11 T cells are depicted in Fig. 11. It is obvious from the bigger square of 11 T cell and measured that the WNM of the 11 T cell is 450 mV, 8 T cell is 420 mV and for 6 T is 370 mV. The simulation outcome confirms that the WNM of the 11 T cell has 17.78% and 6.67% improvement over 6 T and 8 T cells.

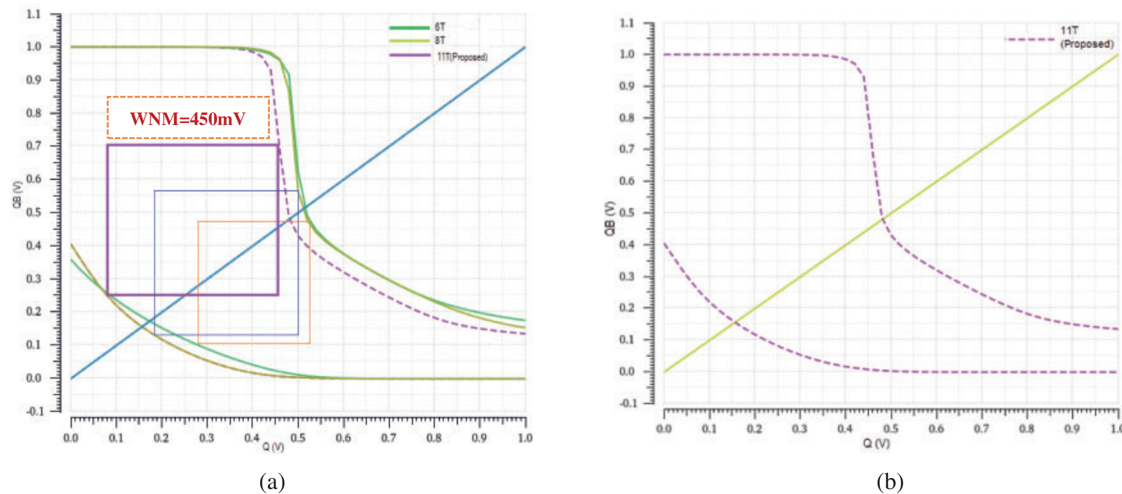


Figure 11: WNM of SRAM cells @ 1 V supply voltage (a) All cells (b) Proposed 11 T cell

4.6 PVT Variations

4.6.1 Process/Voltage/Temperature Variation

The SRAM cells have severe effect on process variations with power dissipation, speed, performance, and stability [32,33]. The process analysis on all process corners i.e., TT (Typical NMOS, Typical PMOS), FF (Fast NMOS, Fast PMOS), FS (Fast NMOS, Slow PMOS), SF (Slow NMOS, Fast

PMOS) and SS (Slow NMOS, Slow PMOS) has been investigated for all the operations. The worst-case variation can be analyzed through corner analysis. The PVT (process, voltage, temperature) variation is performed to determine the propagation time of the transistors. The extreme level of parametric variation can be determined from process corner simulations [34]. The voltage variation is applied from 0.2 V till 1 V to analyze the behavior and performance of cells. The temperature variation is applied from −50°C to 150°C to understand the cell immunity at different environmental conditions.

4.6.2 *Impact of PVT Variation on Write Power and Delay*

Due to inter-die variations, the threshold voltage will always change. Hence, the power, delay, performance and stability are normally affected [35,36]. The write power and write delay simulation results at all the process corners are reported in Tab. 8. The Figs. 12 and 13 show the voltage and temperature variation for write power and delay. The proposed cell performs better in all the corners compared to other cells and improves the write ability. The proposed cell's average power and delay for write operation is lesser compared to other cells.

Table 8: Write power and delay analysis of SRAM cells at different process corners

Process corners	Write power (nW) of cells					Write delay (pS) of cells				
	6 T [20]	8 T [21]	10 T [22]	11 T [23]	11 T (proposed)	6 T [20]	8 T [21]	10 T [22]	11 T [23]	11 T (proposed)
TT	32.004	34.565	8.856	14.506	18.234	343.66	402.15	422.56	722.51	252.73
FF	44.000	47.095	9.958	21.250	23.112	303.45	354.56	190.99	451.06	217.13
SS	22.260	24.551	7.168	16.912	14.087	389.22	459.24	1138.8	1042.3	288.78
FS	29.397	31.845	17.853	15.038	16.792	276.52	341.26	670.08	510.60	197.95
SF	33.222	35.766	7.117	20.774	19.610	405.54	458.98	343.09	975.89	303.97

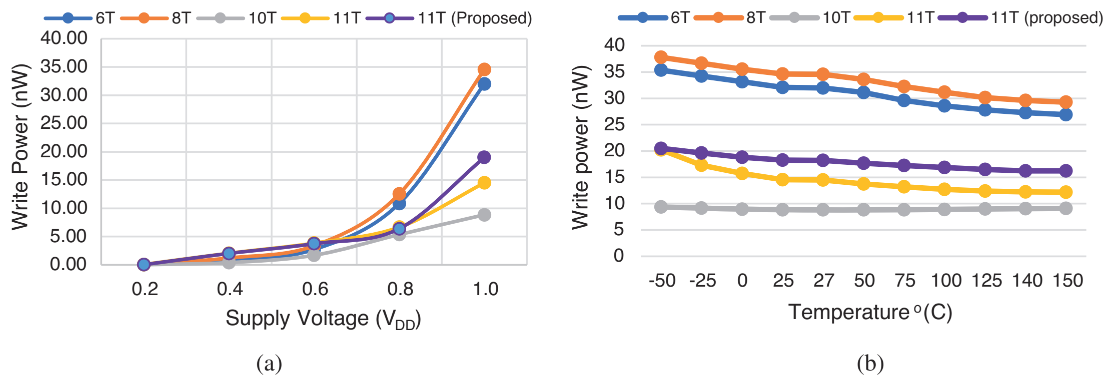


Figure 12: Variation analysis of write power (a) Supply voltage variation (b) Temperature variation

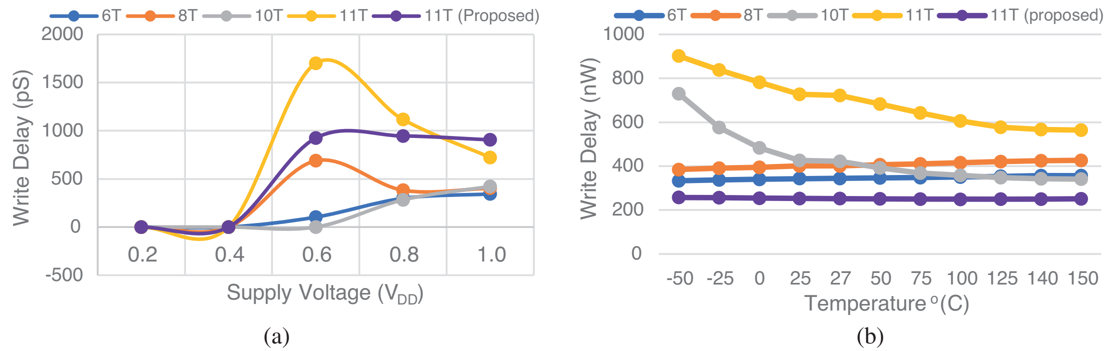


Figure 13: Variation analysis of write delay (a) Supply voltage variation (b) Temperature variation

4.6.3 Impact of PVT Variation on Read Power and Delay

The read power and read delay simulation results at all the process corners are presented in Tab. 9. The voltage and temperature variation results for read power and delay are plotted in Figs. 14 and 15. The proposed cell becomes faster in higher voltages and same time this causes the minimum effect of variation and increases the read stability. The proposed cell is stable and can be used in any suitable environment settings/conditions and perfectly works for V_{DD} as low as 400 mV without any degradation. The average read delay of the suggested 11 T cell is comparatively less and stability is improved in all corners.

Table 9: Read power and delay analysis of SRAM cells at different process corners

Process corners	Read power (nW) of cells					Read delay (pS) of cells				
	6 T [20]	8 T [21]	10 T [22]	11 T [23]	11 T (proposed)	6 T [20]	8 T [21]	10 T [22]	11 T [23] (nS)	11 T (proposed)
TT	70.716	71.023	13.210	59.224	48.707	236.10	93.65	430.05	100.91	116.54
FF	90.190	90.274	21.015	73.506	61.379	256.12	50.56	373.62	100.95	71.50
SS	56.200	58.471	5.910	50.023	35.977	557.79	165.52	551.20	100.85	177.88
FS	69.024	69.048	16.920	58.311	49.365	40.44	47.16	309.66	100.81	74.94
SF	69.120	69.843	9.425	57.556	42.158	377.45	141.40	565.50	100.95	162.45

4.6.4 Impact of PVT Variation on Static Power

The simulation results of static power variations are plotted in Fig. 16. With the increase of temperature, the static power normally increases [37]. The variation of temperature will affect the speed of the cell [38]. The average static power is less compared to other cells in process variation due to the stack effect of the tail transistors. The static power is about 42% less in different temperature variation analysis compared to 6 and 8 T cells.

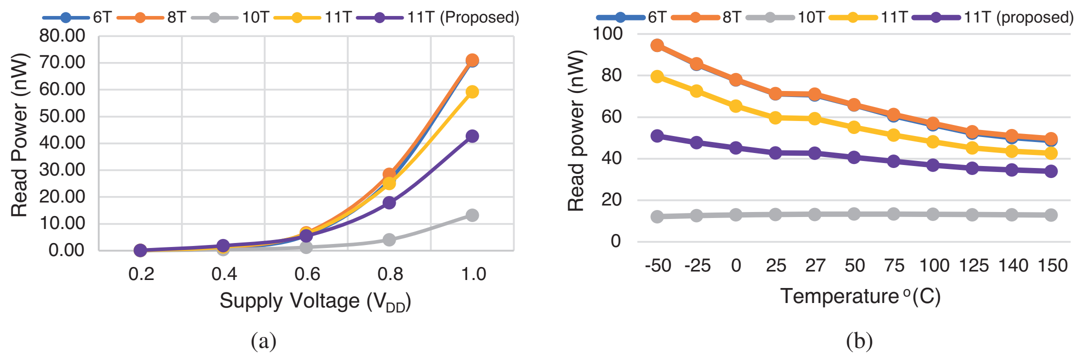


Figure 14: Variation analysis of read power (a) Supply voltage variation (b) Temperature variation

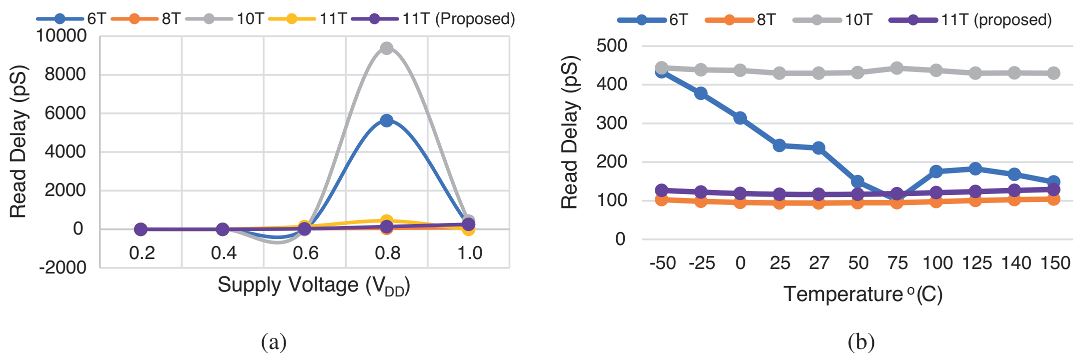


Figure 15: Variation analysis of read delay (a) Supply voltage variation (b) Temperature variation

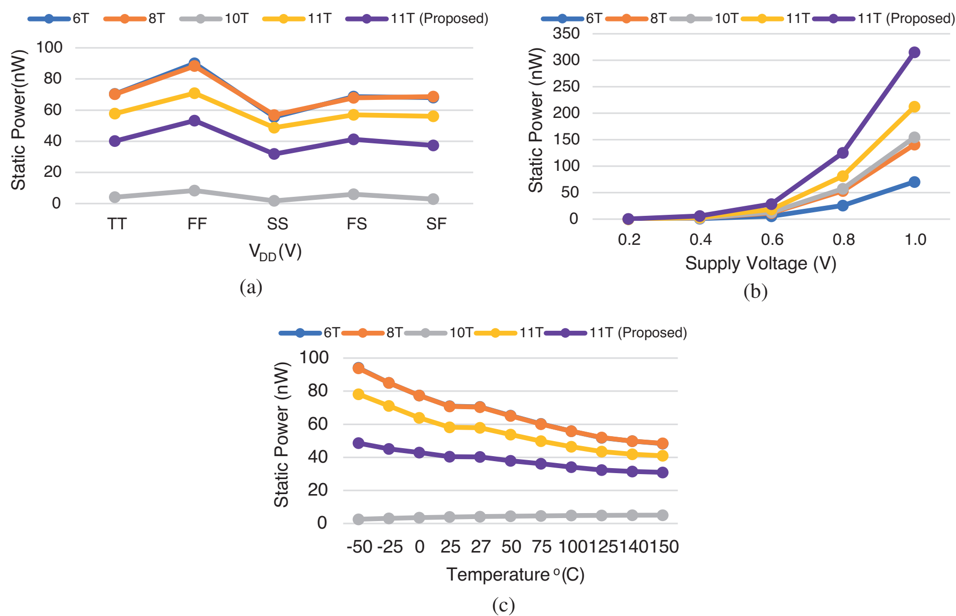


Figure 16: Variation analysis of static power (a) Process corners (b) Supply voltage (c) Temperature

4.7 Statistical Variability Analysis of the Proposed Cell

The Monte Carlo (MC) analysis is carried out to evaluate the proposed cell's effectiveness and robustness at $V_{DD} = 1$ V for all three operations. The Gaussian distribution with 3σ variation of 10% is applied while carrying out the MC simulation on 5000 samples for all operations. The statistical outcome and distribution for write and read power is plotted in Fig. 17. The mean (μ) and standard deviation (σ) of power and delay with respect to process and mismatch variations are presented in Tabs. 10 and 11. It can be inferred from the table that the mean write power of proposed cell is 42% and 47% less and mean read power is less by 31% over 6 T, 8 T and 18% against 11 T cells. The variability (σ/μ) is also calculated and presented for power and delay of all cells at 1 V.

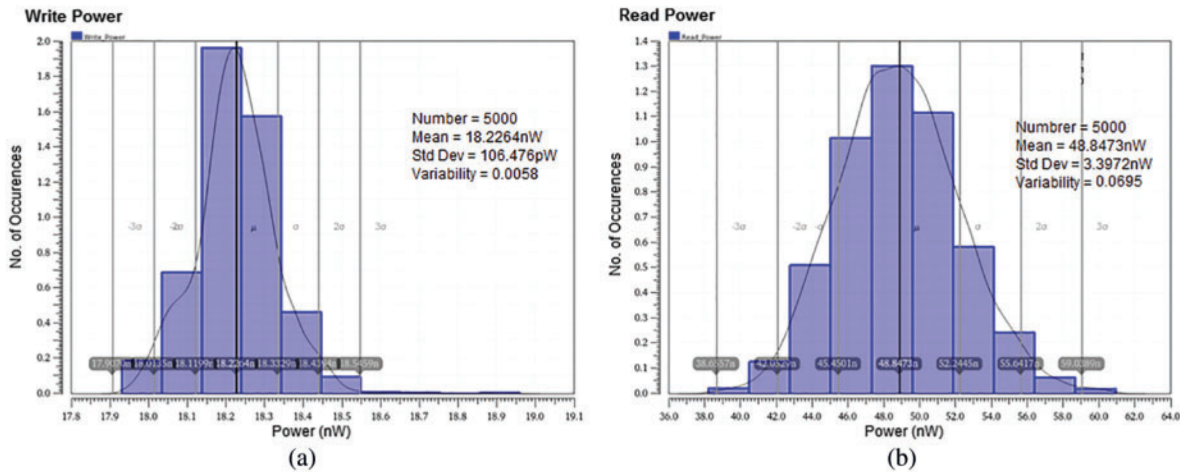


Figure 17: The 5000 MC simulation of proposed cell (a) Write power (b) Read power

Table 10: Write/read power variability analysis of different cells (5000 samples)

No	SRAM cells	Number of samples	Write power			Read power		
			Mean (nW)	Standard deviation (nW)	Variability	Mean (nW)	Standard deviation (nW)	Variability
			(μ)	(σ)	(σ/μ)	(μ)	(σ)	(σ/μ)
1	6 T [20]	5000	31.93	1.232	0.0386	70.81	1.677	0.0237
2	8 T [21]	5000	34.32	1.856	0.0541	71.08	1.395	0.0196
3	10 T [22]	5000	10.97	6.819	0.6216	13.32	1.368	0.1027
4	11 T [23]	5000	14.55	0.669	0.0460	59.37	0.694	0.0117
5	11 T (proposed)	5000	18.23	0.107	0.0058	48.85	3.397	0.0695

Table 11: Write/read delay variability analysis of different cells (5000 samples)

No	SRAM cells	Number of samples	Write delay			Read delay		
			Mean (pS)	Standard deviation (pS)	Variability	Mean (pS)	Standard deviation (pS)	Variability
			(μ)	(σ)	(σ/μ)	(μ)	(σ)	(σ/μ)
1	6 T [20]	5000	343.3	13.03	0.0380	235.8	35.86	0.1521
2	8 T [21]	5000	402.3	34.31	0.0853	74.4	1.44n	-
3	10 T [22]	5000	477.0	183.70	0.3851	430.5	24.03	0.0558
4	11 T [23]	5000	725.2	37.49	0.0517	100.9n	1.56	0.0000
5	11 T (proposed)	5000	252.7	7.35	0.0291	116.5	5.16	0.0443

The process tolerance of the cells is evaluated by using the power variability as one main parameter [39,40]. The variability comparison of 11 T and others are presented in Tabs. 10 and 11. It is noted from the table that variability of 11 T cell is 0.0058 for write and 0.0695 for read mode which is significantly less against other cells. Overall, the lower variability (σ/μ) exhibited by proposed cell against other cells on random variation affirms that the cell is robust enough for any suitable applications [41,42].

4.8 Cell Area Considerations

The Fig. 18 shows the layout of suggested 11 T and 6 T cells drawn in 45 nm CMOS technology with its due design rules. The layouts for all the literature cells have been designed and tested with design rule check (DRC) rules and upon checking layout *vs.* schematic (LVS) connections, the RC extraction is carried out. The proposed cell exhibits 2.42x area overhead against normalized area of 6 T cell. The other cells show additional area of 1.24x, 1.72x and 1.68x for 8 T, 10 T and 11 T cells.

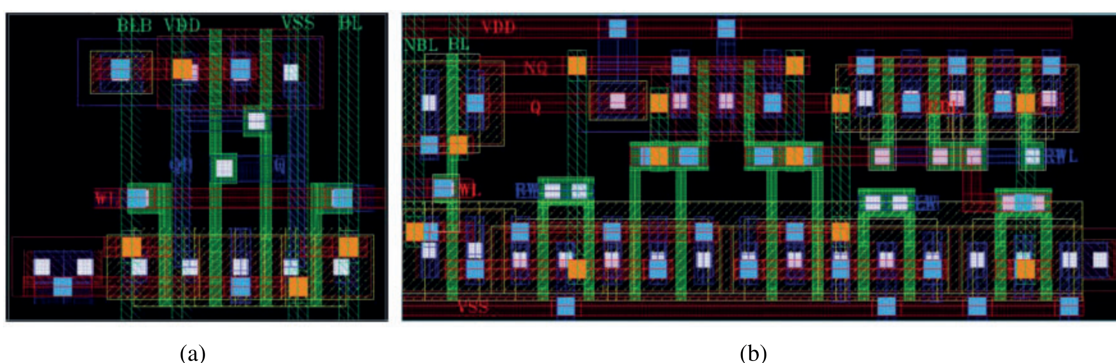


Figure 18: Layout diagram (a) 6 T SRAM cell (b) Proposed 11 T cell

Table 12: Comparison of various parameters of all the cells

	Parameters	6 T [20]	8 T [21]	10 T [22]	11 T [23]	11 T (proposed)
Power	Write power (nW)	32.0043	34.5653	8.8557	14.5061	18.2340
	Read power (nW)	70.7157	71.0227	13.2101	59.2244	48.7065
	Write current (nA)	21.0656	22.7555	2.6254	10.0197	15.7602
	Read current (nA)	97.0769	111.5110	2.8685	112.8450	120.1040
Stability	HSNM (mV)	400	400	-	-	400
	RSNM (mV)	160	345	-	-	460
	WNM (mV)	370	420	-	-	450
Speed	Write delay (pS)	343.658	402.153	422.555	722.505	252.733
	Read delay (pS)	236.095	93.655	430.049	-	116.539
PDP	Write PDP (aJ)	10.999	13.901	3.742	10.481	4.608
	Read PDP (aJ)	16.696	6.652	5.681	-	5.676
Area	Normalized	1	1.24	1.72	1.68	2.42
	Supply voltage (V)	1	1	1	1	1

5 Conclusion

In this research paper, process tolerant and power efficient 11 T SRAM cell is presented and compared with other cells with respect to power, current, delay, stability and area overhead. The cell uses core latch property for write operation and single ended read approach for improving RSNM. The results of various comparative parameters of the cells are summarized in Tab. 12. The WPDP and RPDP are lower by 0.17x, 2.02x and 1.94x, 1.39x against 6 T and 8 T cells that shows the proposed cell is energy efficient with significant process tolerance with variations. The proposed cell is also analyzed in terms of PVT variation as well as MC simulation on 5,000 samples to see the statistical variation. The 0.0058 and 0.0695 variability of the cell for write and read power is less against other cells. The MC simulation and variability analysis outcome validates the efficiency and robustness of the proposed cell without any degradation. The cell exhibits an average lower power of 45%, 33% and improved delay of 32%, 19% for write and read operations over 6 T and 8 T cells in all process corners. The cell also behaves stable at all varying supply voltage and temperature. Thus, PVT analyses affirm that 11 T cell

is highly immune to process variation and environmental conditions. In conclusion, the proposed 11 T SRAM cell design is highly appropriate and an ideal choice for Internet of Things applications.

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