

FPGA Implementation of 5G NR Primary and Secondary Synchronization

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Received: 07 July 2021; Accepted: 22 March 2022

Abstract: The 5G communication systems are widely established for highspeed data processing to meet users demands. The 5G New Radio (NR) communications comprise a network of ultra-low latency, high processing speeds, high throughput and rapid synchronization with a time frame of 10 ms. Synchronization between User Equipment (UE) and 5G base station known as gNB is a fundamental procedure in a cellular system and it is performed by a synchronization signal. In 5G NR system, Primary Synchronization Signal (PSS) and Secondary Synchronization Signal (SSS) are used to detect the best serving base station with the help of a cell search procedure. The paper aims to determine the Physical Cell Identity (PCI) by using primary synchronization and secondary synchronization blocks. The PSS and SSS detection for finding PCI is implemented on Zyng-7000 series Field Programmable Gate Arrays (FPGA) board. FPGA are reconfigurable devices and easy to design complex circuits at high frequencies. The proposed architecture employs Primary Synchronization Signal (PSS) and Secondary Synchronization Signal (SSS) detection aims with high speed and low power consumption. The synchronization blocks have been designed and the synthesized design block is implemented on the Zynq-7000 series Zed board with a maximum operating clock frequency of 1 GHz.

Keywords: 5G new radio; FPGA; physical cell identity; primary and secondary synchronization

1 Introduction

The 5G New Radio communication is the fifth generation of wireless technology for a new radio interface and radio access technology for cellular networks and is developed by 3GPP. It is termed for very high speed, ultra-low latency communications, and also millimeter-wavelength signals. The most vital element for the recent 5G networks is that they should be embedded with low power, high speed, and less area design models. The 5th Generation NR provides a wide range of communications among multimedia, signal processing, image processing, IoT applications, machine-to-machine communications, etc. [1]. All these communication applications involve signal processing with a high data rate and high throughput for a proper transfer of information. The 5G New Radio is



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a millimeter-wave that ranges to 10 ms length [2] frame structure and Orthogonal Frequency-Division Multiplexing (OFDM) technology similar to the Advanced Long Term Evaluation frame but the operating frequency is very high compared to the Long Term Evaluation (LTE). The Orthogonal Frequency Division Multiple Access (OFDMA) signal is highly sensitive to synchronization error, which results in the Inter-Carrier Interface (ICI). Therefore UE needs DL synchronization to protect the orthogonality between sub-carriers and wipe off ICI. The important aspect of 5G New Radio communication is the synchronization of the signals to identify the base station Physical Channel Identity (PCI) which provides the strongest signal [3]. The synchronization of the signals should be very rapid and efficient and thereby the communication will be effective between the sender and the receiver end [4].

The principle of synchronization and the frame structure is studied in detail in the forthcoming sections. The 5G New Radio communications require an efficient model for the synchronization of the signal to determine the cell identity [5]. The cell identity is used to determine the channels, strategy to handover signal, and also the selection of signal with the highest signal strength. The synchronization mainly involves two steps: primary synchronization and secondary synchronization. These synchronization modules enable the user to receiver the perfect signal so that the information conveyed will be significant. In this paper, the algorithm and concepts of Primary synchronization and Secondary synchronization are discussed and the Cell search method is implemented using these synchronization blocks for the 5G New Radio framework [6,7]. The architecture is described by using Hardware Discription Language (HDL) in Xilinx VIVADO 2016.4 and implemented on the Zynq-7000 series Zed board. The sampling frequency of the signals is the specified clock frequency of the implemented synchronization model.

2 5G Frame Structure

The 5G New Radio frame comprises 10 ms as shown in Fig. 1 below. The 10 ms time frame is subdivided into 10 subframes each of the 1 ms time frame. This is a generalized structure for LTE of a 1 ms frame [3]. The sub-frame is mathematically defined as shown in Eq. (1).



OFDM Symbol Duration(us)

 $1ms/2^{\mu}14$

Symbol

(1)



Min= 4.17

Max= 66.67

Cyclic Prefix Duration (us)

Min=0.29

Max= 4.69

Each sub-frame is again divided as slots and each sub-frame has 14 slots [8]. The slot is further divided as symbols, which constitutes a very little space in the entire framework of 10 ms. The mathematical definition for the frame is given as

 $Frame = Subclass = 2 \mu * 14 * 10$

When the sub carrier spacing $\mu = 2$, then

1 symbol = 10 sub-symbols

1 sub-symbols = 2μ spacing = 2 spaces

1 space = 14 OFDM images

Thereby the symbol = 2*10*14 = 280 OFDM images [9]. Thus the OFDM images are adaptive for the 5G New Radio time frame and hence significantly show up with high frequencies with very short symbols i.e., millimeter waves. For example, the 15 kHz symbol in LTE is equivalent to the 2 μ *15 kHz in the 5G New Radio time frame [10]. The numerology support for the 5G New Radio frame is shown in Tab. 1 as below and The subcarrier spacing for various frequencies is represented pictorially mentioned in Fig. 2.

Table 1: Numerology support for 5G NR

 $\Delta f = 2 \mu * 15[kHz]$ Cyclic-prefix μ 0 15 Normal 1 30 Normal 2 60 Normal, extended 3 120 Normal Normal 4 240

No.of slots **Carrier Spacing** 1ms per subframe Sub Frame 1 slot/1ms 15 KHz 1 Slot 0 1 slot/0.5ms 30 KHz 2 Slot 0 Slot 1 1 slot/0.25msis 60KHz 4 Slot 0 Slot 1 Slot 2 Slot3 1 slot/0.125ms 120KHz 0 1 2 • • • 8 8 1 slot/0.0625ms €-> 0 1 2 3 . . . 16 16 240KHz

Figure 2: Sub carrier spacing of 5G NR

(2)

3 Overview of Physical Layer

The overview of the Radio Protocol in the 5G New Radio frame structure is described in this section.

3.1 Physical Layer of 5G NR

The Physical Layer is the top layer in the 5G New Radio hierarchy. It comprises of MAC layer and Resource Layer. The MAC is provided with the transport channel which takes the responsibility of logical channel allocation and the shipping channel is provided with the radio resource channel [11]. The rate of data transferred will purely depend on the logical channel specs.

3.2 Medium Access Layer

The MAC layer is responsible for the controlling of the hardware which is associated with wired, wireless, and optical communications [12,13]. The MAC layer has a tract of vital signals such as clock and reset. It generally operated at a frequency of 20 MHz and is interfaced with the CRC. Fig. 3 shows the Physical Layer frame of the Radio protocol.



Figure 3: Radio protocol architecture around the physical layer

4 5G Beam Management and PCI

The beam management for the synchronization in 5G New Radio will provide access to the user to connect with the gNB in the physical layer and establish the radio link in the physical layer for the UE communication [8]. The beam management constitutes of these operations sweeping, determination, measurement, and reporting of the beam. These operations are defined in Fig. 4.

The initial access to the signal is carried by the primary synchronization block and then it is further handed over to the secondary synchronization block [14]. The obtained signal is considered as the final cell ID of the transmitted signal. The New Radio Primary Synchronization Signal (NR-PSS) is detected to acquire the symbol timing, sector cell index and New Radio Secondary Synchronization Signal (NR-SSS) is used for detecting cell sector index. NR-SSS can be identified only after successful detection of the NR-PSS. Down Link (DL) synchronization performance depends on NR-PSS detection at User Equipment (UE). The primary and secondary synchronizations are explained in detail in the next section.



Figure 4: 5G NR synchronization procedure

$$N_{\rm ID}^{\ \ cell} = 3 * N_{\rm ID}^{\ \ (1)} + N_{\rm ID}^{\ \ (2)}$$
(3)

where $N_{ID}^{(1)} \in \{0, 1, \dots, 335\}$ and $N_{ID}^{(2)} \in \{0, 1, 2\}$

The user equipment determines PCI bunch quantity $N_{ID}^{(1)}$ from Secondary SS and actual layer character $N_{ID}^{(2)}$ from Primary SS mentioned in Fig 5.



Figure 5: Procedure for determining PCI (Physical Cell Identity)

5 Procedure for PSS and SSS

5.1 Primary Synchronization Signal

PSS is constantly positioned in the principal OFDM image of synchronization block [15] and possesses subcarriers with lists from 57 to 183 as proven in Fig. 6.



Figure 6: 5G NR Time-Frequency structure of SSB

The PSS block is configured with the correlation modules followed with the PSS maximum finder [16] and finally the $N_{ID}^{(2)}$ is obtained as shown in Fig. 7. 5G-NR Primary Synchronization Signal (PSS) is Physical Layer specific signal and help UE to get Radio Frame Boundary.



Figure 7: 5G NR Primary synchronization signal detection top block

For NR-PSS detection: The matched filters are used for autocorrelation. The M-sequence is used for constant coefficients for taps in the matched filters.

M-sequence: The M-sequence is the longest non-repeating sequence for the taps of matched filters in PSS. A periodic sequence of symbols is generated by a linear feedback shift register whose feedback coefficients form a primitive polynomial.

The Primary SS are depicted as follows.

Discrete Prolate Spheroidal Sequences-DPSS(n) = 1-2x(m)

$$m = (n + 43 N_{ID}^{(2)} \mod 127)$$

 $0 \le n < 127$

Where

 $x(i + 7) = (x(i+4) + x(i)) \mod 2$

And initial state

[x(6) x(5) x(4) x(3) x(2) x(1) x(0)] = [1 1 1 0 1 1 0]

The maximum correlation signal out of three matched filters will be calculated and the corresponding number is treated as $N_{ID}^{(2)}$.

5.2 Secondary Synchronization Signal

SSS is consistently positioned inside the third OFDM image of synchronization block [17] (like PSS) and involves subcarriers with files from 57 to 183 as appeared in Fig. 8.



Figure 8: 5G NR Secondary synchronization signal detection algorithm

Be that as it may, the 5G NR Primary SS comprises of one among three 336 127-images gold sequence and is assigned at the 3rd image of every Synchronization Signal Block (SSB), and on 127 subcarriers as shown in Fig. 9. The 336 possible Gold sequence for the Secondary SS [18] are portrayed as follows.

$$DSSS = [1 - 2 \times 0 ((n + m0) \mod 127)][1 - 2 \times 1 ((n + m1) \mod 127]$$
(5)

$$\begin{split} m0 &= 15[N_{ID}^{(1)}/112] + 5 N_{ID}^{(2)} \\ m1 &= N_{ID}^{(1)} \mod 112 \\ 0 &\leq n < 127 \text{ Where} \\ X0(|i+7|) &= (X0 (|i+4|) + X0 (i)) \mod 2 \\ X1(|i+7|) &= (X1 (|i+1|) + X1 (i)) \mod 2 \\ And Initial state: \\ [X1(0) X1(1) X1(2) X1(3) X1(4) X1(5) X1(6)] &= [1 0 0 0 0 0 0] \\ [X0(0) X0(1) X0(2) X0(3) X0(4) X0(5) X0(6)] &= [1 0 0 0 0 0 0] \end{split}$$

(4)



Figure 9: 5G NR Secondary synchronization signal detection top block

6 Simulation Results

The simulation results for the proposed synchronization blocks i.e., primary synchronization and secondary synchronization is shown in Figs. 10–15 below.



Figure 10: 5G NR PSS detection top level schematic block

7 Performance Evaluation

Implementation manner is accomplished through using FPGA Zynq-7000 series Zed-board. The utilization reports of post-synthesis of design are given as shown below. The Primary SS Synchronizer and Secondary SS Synchronizer module utilization summary is detailed with respective summary reports. The resource utilization summary for the existing algorithm [1] and the proposed algorithm is tabulated as shown below in Tab. 2.



Figure 11: 5G NR SSS detection top level schematic block



Figure 12: 5G NR PSS detection gate level schematic



Figure 13: 5G NR SSS detection gate level schematic



Figure 14: 5G NR PSS detection output waveform



Figure 15: 5G NR PSS & SSS implemented design

Technique	Resource	Utilization	Available	Utilization (%)
Traditional	LUT	23075	78600	29.36
algorithm [1]	LUT RAM	48	26600	0.18
	FF	10679	157200	6.79
	DSP	400	400	100
	ΙΟ	93	250	37.20
	BUFG	1	32	3.13
Chunjing algorithm	LUT	10680	78600	13.59
[1]	LUT RAM	48	26600	0.18
	FF	14415	157200	9.17
	DSP	0	400	0
	IO	93	250	37.20
	BUFG	1	32	3.13
Proposed algorithm	LUT	1442	53200	2.71
	LUT RAM	0	17400	0
	FF	16	106400	0.015
	DSP	4	220	2
	ΙΟ	47	200	2.35
	BUFG	1	32	9.17

Table 2: Resource utilization of the proposed and existing algorithms

The reports of power consumption and delay are listed in the Tab. 3 as compared with the existing algorithm [18]. Determination of PCI (Physical Cell Identity) mentioned in Tab. 4.

		Existing algorithm	Proposed algorithm
PSS	Delay (µs)	27.148	14.236
	Power consumption (mW)	4.335	1.243
SSS	Delay (µs)	59.813	27.627
	Power consumption (mW)	6.254	2.015

Table 3: Power consumption and delay report

	PSS (NID(2))	SSS (N(1) ID)	PCI (NIDcell = $3 * \text{NID}(1) + \text{NID}(2)$)
Case-1	1	33	100
Case-2	2	32	98
Case-3	2	34	102

 Table 4: Determination of PCI (Physical Cell Identity)

The values obtained by the PSS and SSS correlation [19-21] by considering different cell IDs are plotted graphically as shown below in Figs. 16-21.

Case 1: Calculation of Physical Cell Id (PCI)

NID cell = $3 * N_{ID}^{(1)} + N_{ID}^{(2)}$

$$= 100$$

= 3(33) + 1





Case 2: Calculation of Physical Cell Id(PCI) [22]

$$\begin{split} \text{NIDcell} &= 3* \, N_{ID}^{(1)} + \, N_{ID}^{(2)} \\ &= 3(32) + 2 \\ &= 98 \\ \text{Case 3: Calculation of Physical Cell Id(PCI)} \\ \text{N}_{\text{ID}}\text{cell} &= 3* \, N_{ID}^{(1)} + \, N_{ID}^{(2)} \\ &= 3(34) + 2 \end{split}$$



Figure 17: SSS Correlation vs. Frequency offset (PCI=100)



Figure 18: . PSS Correlation vs. Frequency offset (PCI=98)



Figure 19: SSS Correlation vs. Frequency offset (PCI=98)



Figure 20: PSS Correlation vs. Frequency offset (PCI=102)



Figure 21: SSS Correlation vs. Frequency offset (PCI=102)

8 Conclusion

This suggested design of the Primary SS and Secondary SS Synchronizer for 5G NR base-band receiver were validated, verified, and implemented efficiently on an FPGA Zynq-7000 series Zed board. The results show that the proposed design ensures the determination of cell identity effectively by incorporation of the proposed technique of primary and secondary synchronization blocks. Also, the hardware utilization is reduced by 63.7%, power consumption is reduced by 31.2%, and is operated with high speed with a minimum of 200 MHz and a maximum of GHz clock rates.

Funding Statement: The authors received no specific funding for this study.

Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

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