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Cache Memory Design for Single Bit Architecture with Different Sense Amplifiers

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Abstract: Most modern microprocessors have one or two levels of on-chip caches to make things run faster, but this is not always the case. Most of the time, these caches are made of static random access memory cells. They take up a lot of space on the chip and use a lot of electricity. A lot of the time, low power is more important than several aspects. This is true for phones and tablets. Cache memory design for single bit architecture consists of six transistors static random access memory cell, a circuit of write driver, and sense amplifiers (such as voltage differential sense amplifier, current differential sense amplifier, charge transfer differential sense amplifier, voltage latch sense amplifier, and current latch sense amplifier, all of which are compared on different resistance values in terms of a number of transistors, delay in sensing and consumption of power. The conclusion arises that single bit six transistor static random access memory cell voltage differential sense amplifier architecture consumes 11.34 μW of power which shows that power is reduced up to 83%, 77.75% reduction in the case of the current differential sense amplifier, 39.62% in case of charge transfer differential sense amplifier and 50% in case of voltage latch sense amplifier when compared to existing latch sense amplifier architecture. Furthermore, power reduction techniques are applied over different blocks of cache memory architecture to optimize energy. The single-bit six transistors static random access memory cell with forced tack technique and voltage differential sense amplifier with dual sleep technique consumes 8.078 μW of power, i.e., reduce 28% more power that makes single bit six transistor static random access memory cell with forced tack technique and voltage differential sense amplifier with dual sleep technique more energy efficient.

Keywords: Current differential sense amplifier (CDSA); voltage differential sense amplifier (VDSA); voltage latch sense amplifier (VLSA); current latch sense amplifier (CLSA); charge-transfer differential sense amplifier (CTDSA); new emerging technologies

1 Introduction

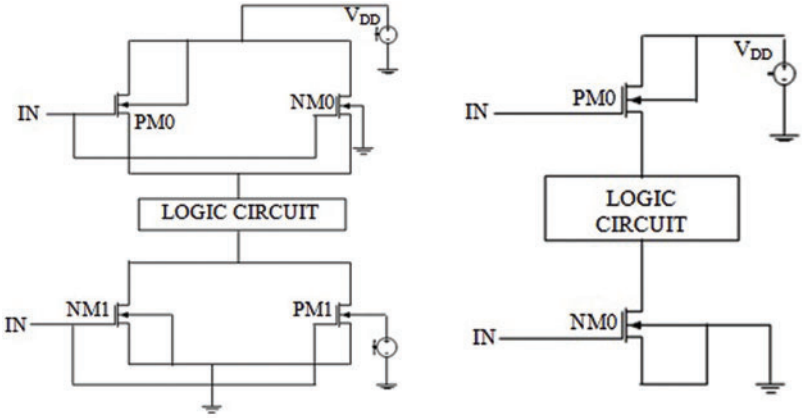
Very-large-scale integrated circuit (VLSI) industries keep getting bigger, and the demand for mobile devices and battery-powered embedded systems is getting bigger and bigger all the time [1]. It takes up 60% to 70% of the chip area. As more chips are used, the speed of microprocessors slows down. Single-chip failure rates go up and down when a million transistors are on each chip. Cache memories now use more than half of a high-performance computer's transistors, which is expected to rise [2]. $6TSRAM_C$ is the most common option for built-in stock because it is vital in chips like this that work well in noisy places. The design of low-power, high-performance processors, on the other hand, was given a lot of attention [3]. At some point, speed and power made things better. SA is an essential part of all $6TSRAM_C$ memory blocks because it responds well to high frequency. It's the same for C_{MOS} memories and other integrated circuits [4]. When there is more memory, the parasite space of the bit line tends to grow. In the last few years, the amount of memory that needs a lot of energy has kept going up. Cache memory is used to speed up synchronizing with a high-speed central processing unit (CPU). It is used as a CPU register because of its economic behaviour, even though it is costlier than the main memory. Cache memory is a buffer between the CPU and (random access memory) RAM, as the memory is high-speed [5]. It has data and instructions to easily and instantly accessible to the CPU. Cache memory is of two types, i.e., $6TSRAM_C$ and dynamic random-access memory (DRAM). $6TSRAM_C$ reduces the average time for data access and has a holding capacity of data than DRAM.

1.1 Low Power Reduction Techniques (LPRT)

This section discusses a small introduction of low power reduction techniques, including the working of techniques in the logic circuit and the working of transistors, as shown below [6].

1.1.1 Low Power Reduction Dual Sleep Technique

Space requirements for this technology are cut down because each transistor is replaced by three transistors, which takes up less space [7]. All logic circuits have a dual sleep component as standard. Schematic 1a illustrates that a specific logic circuit requires fewer transistors.



(a) (b)

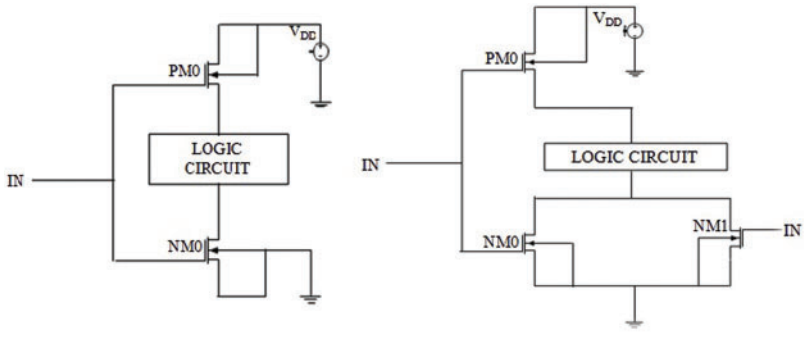
Schematic 1: (a) Low power reduction dual sleep technique circuit diagram, (b) Low power reduction sleep transistor technique circuit diagram

1.1.2 Low Power Reduction Sleep Transistor Technique

Low Power Reduction Sleep Transistor Technique is a well-known technique. It is also known as Power Reduction MTC_{MOS} Technique. Schematic 1b [8] shows an extra sleep PMOS transistor between the V_{DD} and the circuit pull-up network.

1.1.3 Low Power Reduction Forced Stack Technique

In the forced stack approach, instead of using a voltage supply, PM0 is utilized in the logic circuit, and instead of ground, NM0 is used, as illustrated in the Schematic 2a. Both MOS has the same input in this approach [9].



(a) (b)

Schematic 2: (a) Low power reduction forced stack technique circuit diagram, (b) Low power reduction sleep stack technique circuit diagram

1.1.4 Low Power Reduction Sleep Stack Technique

Schematic 2b illustrates its structure. When both transistors are switched off simultaneously, the resulting reverse bias causes a sub-threshold reduction in leakage current. The sleepy stack approach was solved by integrating sleep and stacking methodologies [10].

Apart from the introduction, Section 2 covers related work in cache memory design for single-bit architecture. Section 3 describes a functional block diagram of cache memory design for single-bit architecture. Section 4 describes the proposed single bit $6TSRAM_C$ SA architecture with its working and schematic. Section 5 describes simulated results with output waveforms and comparisons concerning the consumption of power, delay in sensing, and several transistors. Section 6 describes the summary of the paper in the form of a conclusion and future scope.

2 Literature Review

This section describes related work done in 6TSRAMC till 2022 by different authors' papers. The conclusion arises from Tab. 1 that $6TSRAM_C$ is the most popular in cache memory.

Table 1: Describe related work done by different authors

Authors	Major findings
Zhang et al. [11]	Contextual variables such as cache size and ageing are taken into account. Performance-reliability metrics and embedded microprocessors regression models examine performance reliability.
Roy et al. [12]	Embedded cache memory design factors. Changing process, voltage, and temperature at low supply voltages make building a reliable $6TSRAM_C$ difficult. When employed at a scaled technology node, $6TSRAM_C$ suffer read and write mistakes and instability.
Mittal et al. [13]	Researchers are investigating in-memory computing techniques for $6TSRAM_C$ that might speed up various computer systems and applications. In-memory computing utilizing $6TSRAM_C$ memory is feasible.
Gavaskar et al. [14]	Ad hoc power dissipation is crucial in most electronic systems, leading to various proposals for saving power during the hold, write, and read phases. A complementary metal-oxide-semiconductor integrated circuit's memory is critical. This research will look at low-power and low-voltage $6TSRAM_{Cs}$ for current leakage power.
Aparna [15]	Nowadays, the most extensively utilized memory technology is $6TSRAM_C$. Due to its enormous extent, this memory is crucial. As integration grows, leakage power, current, and delay become challenges in $6TSRAM_C$ design.
Agrawal [16]	$6TSRAM_C$ is used in cache memory, microprocessors, and electrical circuits. Most utilize $6TSRAM_C$. Writing and reading take more power and have a smaller signal-to-noise margin (SNM). Memory cells with transmission gates offer better write margins than other technologies.
Dinesh Kumar et al. [17]	Wearable and implantable biomedical technology can now read biosignals and measure changes. Devices connected to the cloud may help solve problems more quickly. It must be shared between memory and processor to be used. To respond quickly, the superior processor needs data from its memory.
Neeraj et al. [18]	This is one possible answer to current memory issues. More efficient, faster, and easier to extend memory. Circuits may save energy by using embedded memory like $6TSRAM_C$.
Kamaraju et al. [19]	Today's gadgets are capable of meeting user requests. Many widgets have a memory that grows with the device. Everyone wants inexpensive and fast computers. $6TSRAM_C$ is the most extensively used memory cell due to its superiority.

(Continued)

Table 1: Continued

Authors	Major findings
Siva Kumar et al. [20]	As technology advances, more people use devices to store and analyze vast volumes of data. The speed of a 6TSRAM$_C$ is appealing. Using more memory cells uses more power. 6TSRAM$_C$ has to be improved for object tracking memory cells.
Soong et al. [21]	The evolution of on-chip 6TSRAM$_C$ memory has altered considerably. Wireless sensor networks (WSNs) and the internet of things (IoT) are gaining popularity, necessitating on-chip data processing. Modern systems rely on low-power, high-performance 6TSRAM$_C$ for their efficiency.
Kim et al. [22]	Artificial intelligence applications like self-driving cars and IoT are becoming more powerful and faster. 6TSRAM$_C$ artificial intelligence architectures are already in use and are accurate. Because complex artificial intelligence models need much power and space, these 6TSRAM$_{Cs}$ have difficulties.
Radhika et al. [23]	Researchers include the standard 6 and 7 T SRAM$_{Cs}$ and the 8 and 9 T SRAM$_{Cs}$, both new. Finally, the 10 T SRAM$_C$ always has the least spillage force and a minor spillage current. This improves readability compared to the 6, 7, 8, 9, and 10 T SRAM$_{Cs}$.
Liu et al. [24]	Their outstanding bandgaps for ultra-small logic transistors make MoS_2 and WSe_2 ideal for ultra-small logic transistors. Monolayer 2DM 6TSRAM$_{Cs}$ read and write quicker than the other two types.
Wang et al. [25]	Currently, VLSI circuits are in great demand. A more efficient C$_{MOS}$ circuit consumes less power. Moore's law claims that chip transistor count doubles every two years. Devices are smaller and more densely bit line, and bit line bar write and read.
Gupta et al. [26]	Leakage-reduction techniques in 6TSRAM$_{Cs}$ are broken down into three groups: latch, bit line, and read port. Multi-threshold C$_{MOS}$ is found to be the best way to cut down on latch leaks.
Krishnaraj et al. [27]	They are dense and may operate with typical C$_{MOS}$ processes, allowing single-chip CPU/main memory designs. However, space constraints make combining a multi-core CPU and central memory system challenging.
Huang et al. [28]	Practically all embedded machinery and industries now rely on IoT-enabled apps. IoT devices need a lot of memory to store photos, videos, and music. DRAM uses a capacitor, requiring more power and large updating circuits. The new 6TSRAM$_C$ divides read and write operations and uses sleep transistors to save power and time.
Kumar et al. [29]	6TSRAM$_C$ has been the most extensively utilized memory type for a decade. So long as the power is on, the data may be stored. It's a kind of RAM that uses latching circuitry to store data. 6TSRAM$_C$ is a critical component of computer memory.

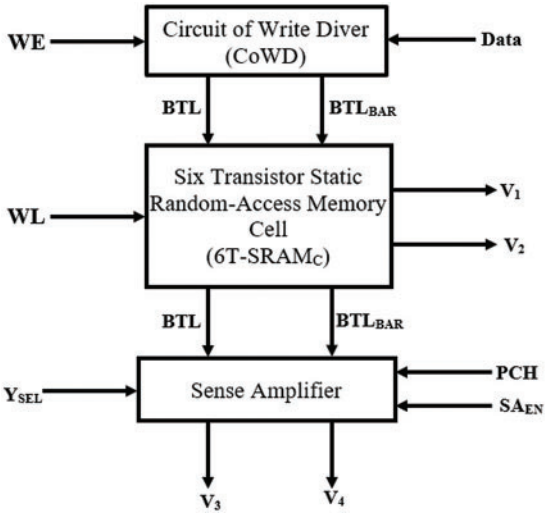
(Continued)

Table 1: Continued

Authors	Major findings
Nouripayam et al. [30]	With the rise of technology and the scaling factor, the amount of power used at rest must be reduced. So, a 6TSRAM$_C$ wants new techniques and architecture to run at very low sub-threshold voltages.

3 Cache Memory Design for Single Bit Architecture

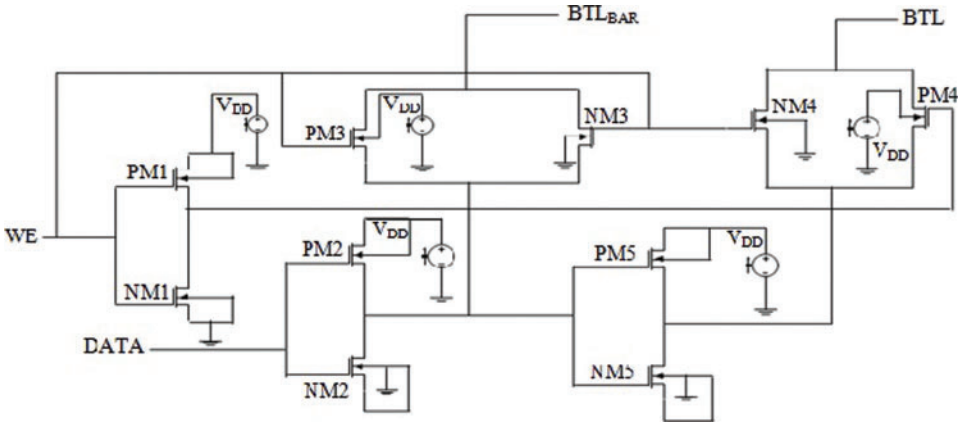
They are creating a cache memory for single-bit architecture that allows for non-destructive reads and reliable writes. These two requirements collide when it comes to the size of 6TSRAM$_C$ transistors. 6TSRAM$_C$ transistor ratios must be followed for ad writing to be read successfully [31–33]. The main building blocks of the architectural blocks of ingle bit cache memory are described below. Schematic 3 shows the block diagram of cache memory design for single bit architecture.



Schematic 3: Block diagram of cache memory design for single bit architecture

3.1 Circuit of Write Driver (CoWD) Working and Schematic

The CoWD function of the 6TSRAM$_C$ circuit is to rapidly discharge one of the bit-lines from pre-charge levels to below the 6TSRAM$_C$ write margin. Write Enable (WE) signal activates CoWD, which uses full-swing discharge to drive the bit line from the pre-charge stage to the ground [34]. As illustrated in Schematic 4, the order in which word line (WL) is authorized and CoWD is triggered is unimportant for the proper writing process.

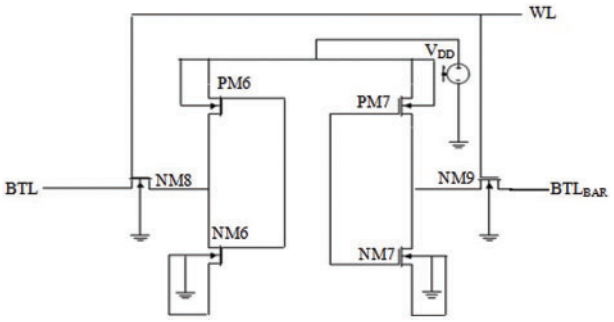


Schematic 4: CoWD circuit diagram

3.2 Six-Transistor Static Random Access Memory (6TSRAM$_C$) Working and Schematic

The design of 6TSRAM$_C$ is essential for the safe and robust functioning of the architecture. The 6TSRAM$_C$ must be small, stable, robust, and yield constraints—binary data storage by a 6TSRAMC portion [35]. The word line defines modes of operation. When all transistors are removed, and cells are separated. The word line pulls high for reading and writing functions that enable access transistors (NM8 and NM9).

A typical 6TSRAM$_C$ uses two cross-connected inverters, which create a transistor lock and access [36]. Access transistors (NM8 and NM9) allow reading and writing to the cell and provide cell isolation when the cell is not accessible, as shown in the Schematic 5.



Schematic 5: 6TSRAM$_C$ circuit diagram

3.3 Sense Amplifiers (SA's)

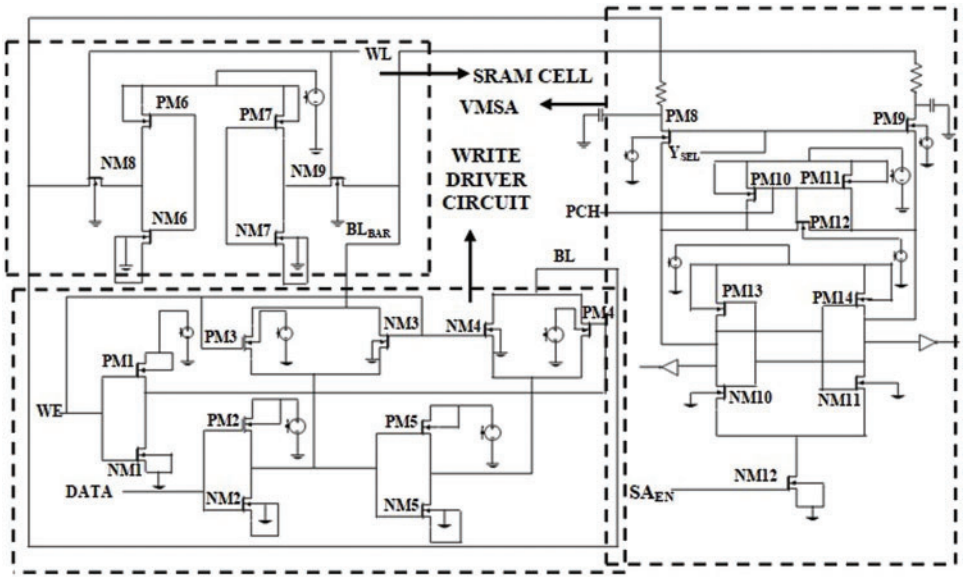
SA is a vital memory design aspect. SA's preference and configuration determine the robustness of bit-line detection, which impacts readability and power [37–39]. Sensing operation must be non-destructive, provided that 6TSRAM$_{Cs}$ need no data to refresh circuits after sensing.

4 Proposed Single Bit 6TSRAM$_C$ SA Architecture

In this section, all the proposed architecture schematic has been shown as well as the working of all the architecture has been defined below [40].

4.1 Single Bit 6TSRAM$_C$ VDSA Architecture Working and Schematic

Voltage Differential Sense Amplifier (VDSA) detects the bit-line differential voltage and generates a total rail output. The circuit is depicted in Schematic 6. The BTL and BTL$_{BAR}$ pair create a voltage difference when WL = high. When SAEN = high, when the required differential is reached, the cross-coupled inverter enters a positive feedback loop [41].



Schematic 6: Single bit 6TSRAM$_C$ VDSA architecture circuit diagram

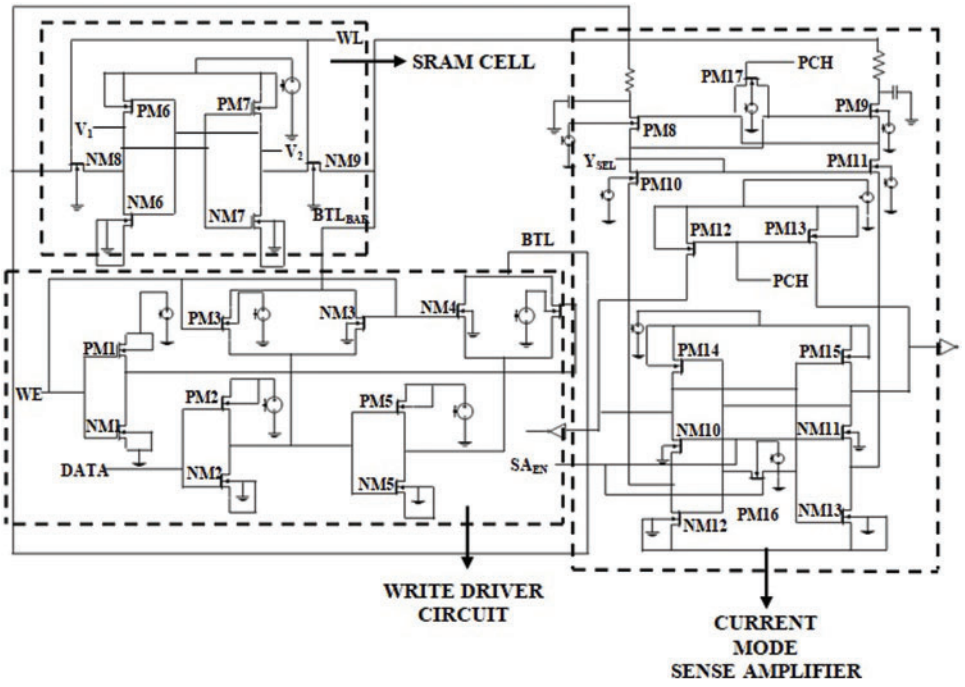
The bit-line connected SA output node is set to zero, while the other output SA_1 is kept raised with a lower voltage, e.g., SA_2. When the sensing amplifier is turned on, NM10 and NM11 become saturated. The NM11 device has a greater V_{DD} input voltage than the NM10, with a lower Vgs voltage. The more significant current (NM11) results in a lower output voltage on the other NM10 device, lowering V_{gs} and resulting in a lower current [42].

4.2 Single Bit 6TSRAM$_C$ CDSA Architecture Working and Schematic

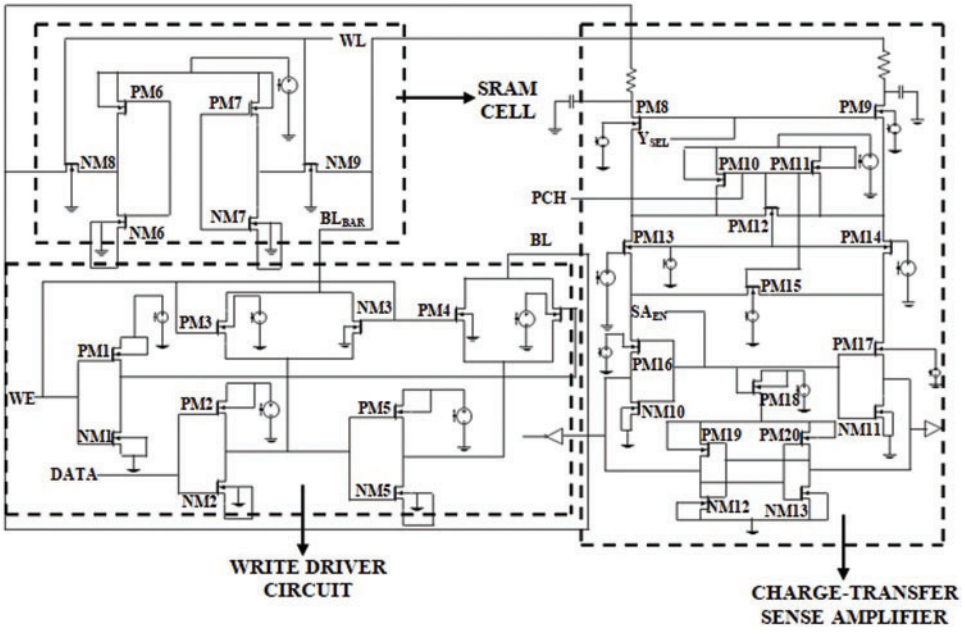
The circuit architecture for a current detecting amplifier is shown in the Schematic 7. CDSA operates by directly measuring bit-cell current. It does not rely on developing a different voltage across the bit-line [43,44]. The lower bit-line can be clamped at a greater voltage in an amplifier voltage sense. As a consequence, bit-line power pre-charge can be minimized. CDSA has two components: a transmitting circuit with unit transmission characteristics and a sensing circuit that monitors the differential current. Pre-charge and assessment are two tasks of the current mode sensing amplifier [45,46].

4.3 Single Bit 6TSRAM$_C$ CTDSA Architecture Working and Schematic

The circuit diagram of a CTDSA is shown in Schematic 8. Load transfer amplification aims to increase voltage gain by utilizing load conservation across capacitive systems [47]. A charge is transferred from high-capacity bit lines to low-capacity amplifier output nodes in the CTDSA. The minimal voltage swing of the bit-lines results in faster speeds and reduced energy usage.



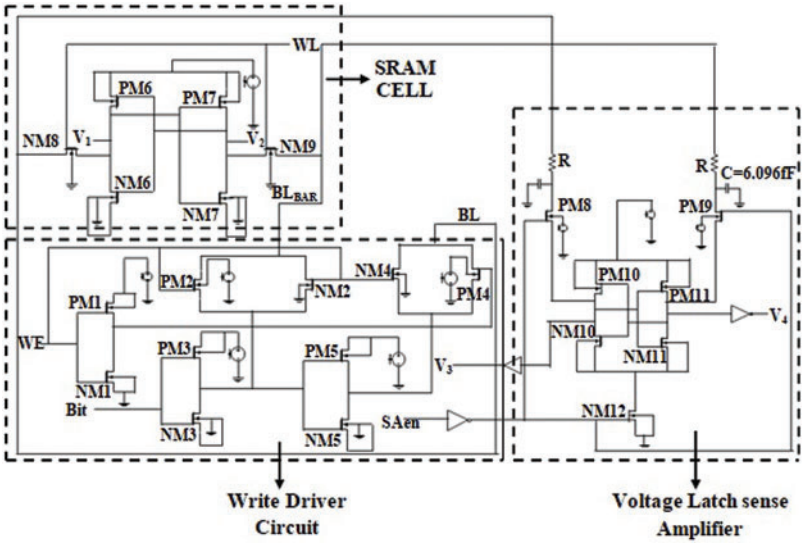
Schematic 7: Single bit 6TSRAM$_C$ CDSA architecture circuit diagram



Schematic 8: Single bit 6TSRAM$_C$ CTDSA architecture circuit diagram

4.4 Single Bit 6TSRAM$_C$ VLSA Architecture Working and Schematic

This study created the voltage latch sense amplifier (VLSA) schematics in this study in Schematic 9. The bit-lines are used to pre-charge the internal nodes of this architecture. The circuit design employs the input bit-lines based on internal nodes [48,49].



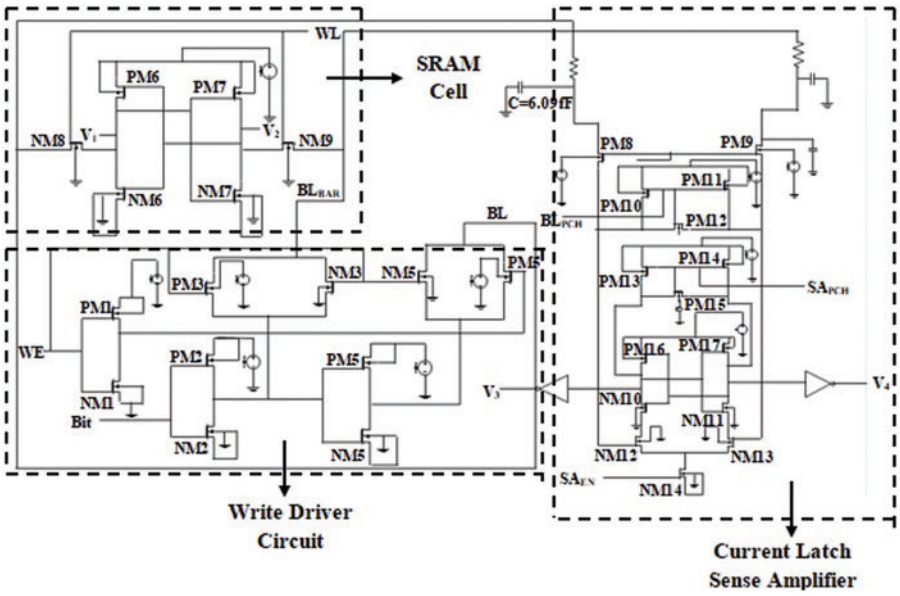
Schematic 9: Single bit 6TSRAM$_C$ VLSA architecture circuit diagram

When the word line is pushed high and before the sense amplifier signal, NM12 is turned off, and PM8 and PM9 pass transistors are turned on. The random bit on the internal nodes of the sense amplifier has an appropriate voltage difference as the differential on the bit lines grows. A differential voltage is amplified to its maximum swing output when the SA_{EN} sensing amplifier signal is asserted [50,51].

4.5 Single Bit 6TSRAM$_C$ CLSA Architecture Working and Schematic

One of the bit lines releases throughout the reading operation, while the other remains at supply voltage. Due to the capabilities of a big bit-line, the slow discharge is moderate, and the bit cells have access to the transistor [52–54].

SA does this by amplifying a slight change in the bit line voltages at digital levels. CLSA schematic is shown in Schematic 10. The differential voltage is carried via bit-lines to the CLSA inputs SA_3 and SA_4. If SA_1 and SA_2 begin to discharge at high levels, SA_{EN} is pulled high [55–58].



Schematic 10: Single bit 6TSRAM$_C$ CLSA architecture circuit diagram

5 Simulation Results

The power consumption of all the circuits has been analyzed in this section. Tabs. 2 and 3 describe a single bit 6TSRAM$_C$ SA architecture with different parameters using different types of SA's such as (VDSA, CDSA, CTDSA, VLSA, and CLSA) at additional values of resistance (such as 42.3 Ω and 42.3 kΩ) with other parameters such as delay in sensing, several transistors and consumption of power.

Table 2: Single bit 6TSRAM$_C$ SA architecture different parameters when C = 6.09 fF, R = 42.3 Ω and V_{DD} = 1.2 V

Architecture	Number of transistors	Delay in sensing	Consumption of power
Single bit 6TSRAM$_C$ VDSA architecture	30	13.51 ηs	13.16 μW
Single bit 6TSRAM$_C$ CDSA architecture	33	18.81 ηs	16.44 μW
Single bit 6TSRAM$_C$ CTDSA architecture	37	18.95 ηs	44.63 μW
Single bit 6TSRAM$_C$ VLSA architecture	29	13.50 ηs	36.57 μW
Single bit 6TSRAM$_C$ CLSA architecture	35	18.68 ηs	73.92 μW

Table 3: Single bit 6TSRAM$_C$ SA architecture different parameters when $V_{DD} = 1.2$ V, C = 6.09 fF, and R = 42.3 KΩ

Architecture	Number of transistors	Delay in sensing	Consumption of power
Single bit 6TSRAM$_C$ VDSA architecture	30	13.51 ηs	11.34 μW
Single bit 6TSRAM$_C$ CDSA architecture	33	18.81 ηs	18.81 μW
Single bit 6TSRAM$_C$ CTDSA architecture	37	18.95 ηs	33.63 μW
Single bit 6TSRAM$_C$ VLSA architecture	29	13.50 ηs	14.32 μW
Single bit 6TSRAM$_C$ CLSA architecture	35	18.68 ηs	26.78 μW

From Tabs. 2 and 3, conclusions arise that singe bit 6TSRAM$_C$ VDSA architecture consumes 11.34 μW of power, the lowest among all the architectures. Due to this reason, LPRT has been applied over a single bit 6TSRAM$_C$ VDSA architecture, but there is an increment in the number of the transistor.

Tab. 4 describes different parameters of single bit 6TSRAM$_C$ VDSA architecture, and to optimize the consumption of power, techniques of power reduction are applied over VDSA. Tab. 5 describes that using LPRT over 6TSRAM$_C$ in single bit 6TSRAM$_C$ VDSA architecture also reduces the consumption of power. Due to this, there is an increment in the number of transistors in the design.

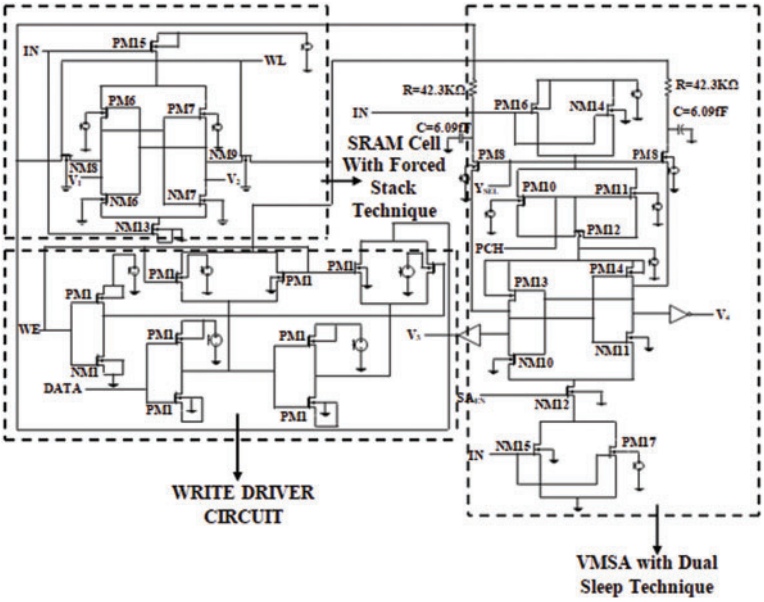
Table 4: Single bit 6TSRAM$_C$ VDSA architecture different parameters when $V_{DD} = 1.2$ V, C = 6.09 fF, and R = 42.3 KΩ on applying LPRT over VDSA in architecture

S. No.	LPRT on VDSA in architecture	Single bit 6TSRAM$_C$ VDSA architecture		
		Number of transistors	Delay in sensing	Consumption of power
1.	LPRSTT	32	13.51 ηs	11.29 μW
2.	LPRFST	32	13.70 ηs	11.29 μW
3.	LPRSST	33	13.50 ηs	11.29 μW
4.	LPRDST	34	13.66 ηs	11.03 μW

Table 5: Single bit 6TSRAM$_C$ VDSA architecture different parameters when $V_{DD} = 1.2$ V, C = 6.09 fF, and R = 42.3 KΩ on applying LPRT over 6TSRAM$_C$ in architecture

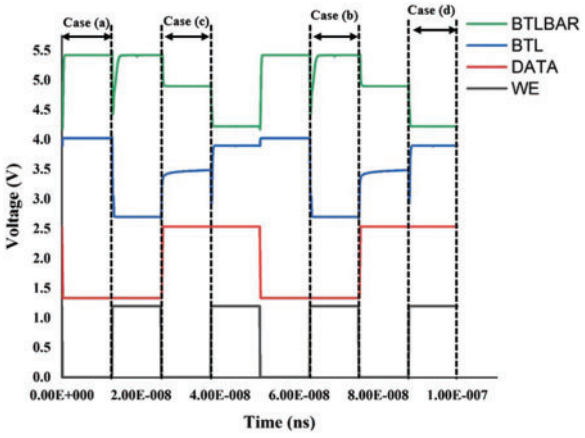
S. No.	LPRT on 6TSRAM$_C$ in architecture	Single bit 6TSRAM$_C$ VDSA architecture		
		Number of transistors	Delay in sensing	Consumption of power
1.	LPRSTT	32	13.12 ηs	9.18 μW
2.	LPRFST	32	13.64 ηs	9.10 μW
3.	LPRSST	33	13.36 ηs	10.38 μW
4.	LPRDST	34	13.51 ηs	10.13 μW

From Tabs. 4 and 5, conclusions arise that Singe Bit 6TSRAM$_C$ with LPRFST VDSA with LPRDST consumes 8.078 μW of power, which is the lowest compared to others. Schematic 11 shows the proposed schematic of single bit 6TSRAM$_C$ with LPRFST VDSA with LPRDST architecture schematic.



Schematic 11: Single bit 6TSRAM$_C$ with LPRFST VDSA with LPRDST architecture circuit diagram

Schematic 12 shows the output waveform of CoWD, where WE and Data are inputs, and BTL and BTL$_{BAR}$ are output are described in four cases.



Schematic 12: CoWD output waveform

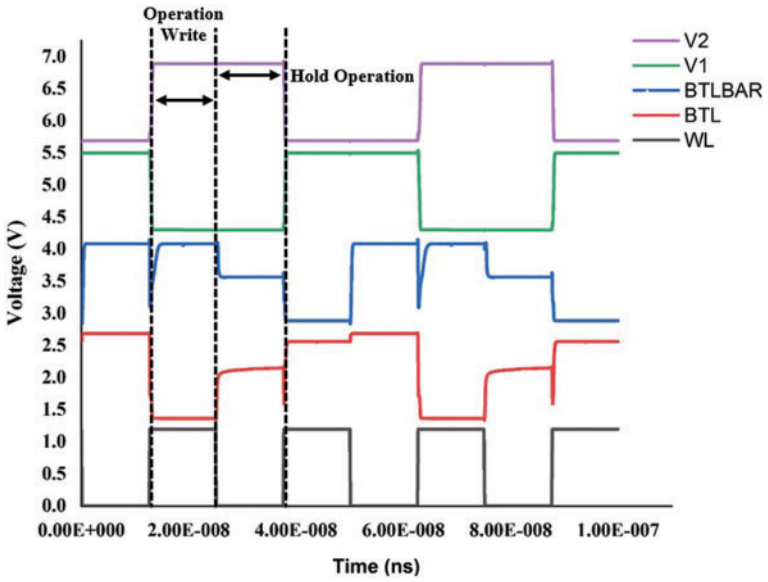
Case (a): WE and Data both are low, BTL and BTL$_{BAR}$ both are high, while,

Case (b): WE are high, Data is low, BTL is low, and BTL$_{BAR}$ is high,

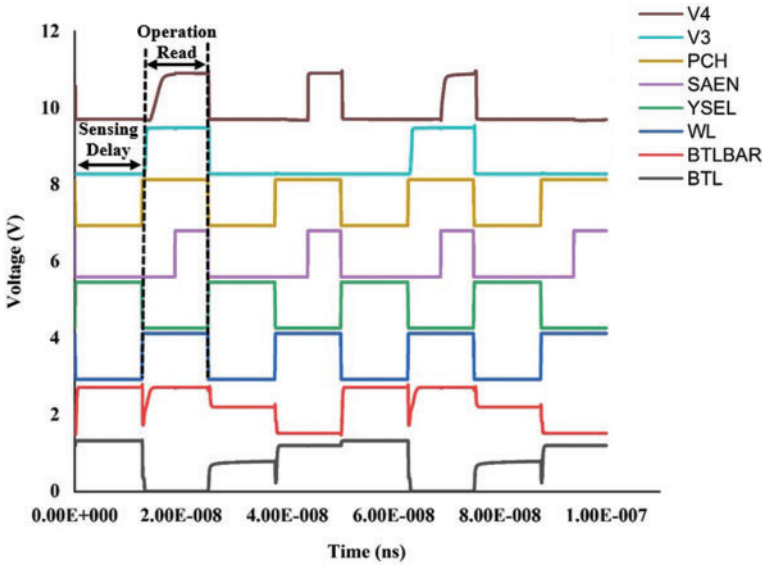
Case (c): Data is high, and WE are low, BTL and BTL$_{BAR}$ are high/2,

Case (d): Data is high, WE are high, BTL is high, and BTL$_{BAR}$ is low.

Schematic 13 shows the output waveform of 6TSRAM$_C$, which shows the write operation and hold operation held in the 6TSRAM$_C$. Schematic 14 shows the output waveform of single bit 6TSRAM$_C$ VDSA architecture, i.e., reading operation done by a SA that reads the store data in 6TSRAM$_C$. Tab. 6 describes applying LPRT over different blocks of cache memory design for single bit architecture (such as 6TSRAMC and VDSA) to optimize power consumption. Results depicted that single bit 6TSRAM$_C$ with LPRFST VDSA with LPRDST architecture consumes 8.078 μW of power which is the lowest as compared to architecture. But due to this, there is an increment in the number of transistors.



Schematic 13: 6TSRAM$_C$ output waveform



Schematic 14: Single bit 6TSRAM$_C$ VDSA architecture

Table 6: Single bit 6TSRAM$_C$ VDSA architecture when C = 6.09 fF and R = 42.3 KΩ on applying LPRT over 6TSRAM$_C$ and VDSA in architecture

S. No.	LPRT over 6TSRAM$_C$ and VDSA in architecture	Single bit 6TSRAM$_C$ VDSA architecture		
		Number of transistors	Delay in sensing	Consumption of power
1.	LPRSTT	34	12.75 ηs	9.27 μW
2.	LPRFST	34	13.14 ηs	9.20 μW
3.	LPRSST	36	12.75 ηs	8.46 μW
4.	LPRDST	38	13.34 ηs	9.74 μW
5.	Single bit 6TSRAM$_C$ (LPRFST) VDSA (LPRDST) architecture	36	12.14 ηs	8.078 μW

6 Conclusion and Future Scope

In this paper, cache memory design for single-bit architecture with different sense amplifiers has been implemented and analyzed. Single Bit 6TSRAM$_C$ SA Architecture comprises CoWD, 6TSRAMC, and SA (VDSA, CDSA, CTDSA, VLSA, and CLSA). All architectures are compared on different values of resistance (R) with other parameters such as consumption of power, delay in sensing and number of transistors. Results showed that single bit six transistor static random access memory cell voltage differential sense amplifier architecture consumes 11.34 μW of power. Furthermore, LPRT is applied over different cache memory architecture blocks to optimize power. The single-bit 6TSRAM$_C$ with LPRFST and VDSA with LPRDST consume 8.078 μW of power, i.e., reduce 28% more ability and make it more efficient.

Future Scope–This work can be done in the form of the array, and LPRT can be applied to other architectures. Moreover, other sense amplifiers can be used in architecture to reduce the drawbacks of the proposed architecture; Apart from it, these architectures can be compared over different parameters such as read delay, write delay, signal to noise margin etc.

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