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Reversible Logic Based MOS Current Mode Logic Implementation in Digital Circuits

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Abstract: Now a days, MOS Current Mode Logic (MCML) has emerged as a better alternative to Complementary Metal Oxide Semiconductor (CMOS) logic in digital circuits. Recent works have only traditional logic gates that have issues with information loss. Reversible logic is incorporated with MOS Current Mode Logic (MCML) in this proposed work to solve this problem, which is used for multiplier design, D Flip-Flop (DFF) and register. The minimization of power and area is the main aim of the work. In reversible logic, the count of outputs and inputs is retained as the same value for creating one-to-one mapping. A unique output vector set can be generated for each input vector set and information loss is also prevented. In reversible MCML based multiplier, reversible logic full adder is utilized to minimize the area and power. D flip-flops based on reversible MCML are often designed to store information that is then combined to form a reversible MCML based register. The proposed reversible MCML multiplier attains average power of 0.683 mW, Reversible MCML based DFF achieves 0.56 μW and Reversible MCML based 8-bit register attains 04.04 μW. The result shows that the proposed Reversible MCML based multiplier, Reversible MCML based D flip-flop and Reversible MCML based register achieves better performance in terms of current, power dissipation, average power and area.

Keywords: MOS current mode logic; reversible logic; multiplier; D flip-flop and register

1 Introduction

The need for very high-speed low-power VLSI circuits is raised due to rapid increase in communication system's transmission speeds [1]. Major two driving forces of this high-speed circuit development are high integration level for providing higher performance with lower cost and provision to implementation with low-power system-on-chip. The CMOS is the popular VLSI technology widely used in recent decades [2]. Although, scaling is used for enhancing CMOS technologies performance in a noticeable manner, applications power and speed requirements cannot be satisfied simultaneously by conventional CMOS circuit. Significant supply noise is generated by conventional CMOS circuits. Sensitive digital and analog circuit's on-chip integration

is hindered by conventional methods. MCML is a logic style, which can satisfy the need of high speed with minimized power consumption when compared with traditional CMOS circuits at these high frequencies [3]. The traditional Emitter Coupled Logic (ECL)'s benefits like common mode noise rejection, di/dt noise minimization, high speed without bipolar transistors requirement can be maintained in MCML. For supply noise, higher immunity is provided by MCML architecture because of its differential structure. Because of its minimized output voltage swing, cross talk is minimized and because of constant current flow in supply rails, noise generation also will be very low. A multiplier is one of the most important building block that is widely used in real-time Digital signal Processing (DSP). Multiplier block should be operated with low power, with minimized layout area while operating at high speed in real-time DSP processing task [4]. Now a days, the multiplier is implemented using both the CMOS [5], MCML logic styles [6] to improve the performance. In the past few decades, most promising research area is reversible logic and in various technologies like optical computing, low power CMOS and nanotechnology, they are used [7]. Garbage outputs count, circuits depth, quantum cost can be reduced by designing reversible logic. The inputs and outputs count are same in these reversible logic circuits. Between output and input vectors, there will be an one to one mapping [8–10]. From inputs, outputs can be computed using this and from outputs, inputs can be recovered uniquely using this. In different digital electronic circuits, to provide proper applications processing, basic units like Memory and registers are made using flip flops. One bit of information can be stored in one flip-flop [11,12]. There are four flip-flop types in basic namely, SR ("set-reset"), T ("toggle"), D ("data") and JK. In these flip-flop types, major difference are inputs count they have and how they change state. For each type, there are also different variations that enhance their operations. The most common flip-flop topology is the DFF [13], however the MCML implementation of a DFF suffers from transparency issues that cause it to act like a latch. Different digital circuits like registers, clock circuits, memory are designed using MOS Current Mode Logic circuits. Recent works are designed multiplier [14], flip flop [15,16] and registers using MOS Current Mode Logic circuits. However, it has only traditional logic gates that have issues with information loss. To overcome this problem, the proposed work integrates the reversible logic with MCML which is used for designing multiplier, D flip-flop and registers. The main contribution of the proposed research work is the reduction of area and power using reversible logic in designed circuits. This paper is structured as follows: Section 1 describes the information about Complementary Metal Oxide Semiconductor, MOS Current Mode Logic, multiplier and flip-flops. Then, Section 2 explains the technical details of the proposed Reversible Logic Based MOS Current Mode Logic Implementation. The simulation results are given in Section 3. Finally, Section 4 concludes this paper.

2 Proposed Methodology

2.1 MCML Based Multiplier Design

The MCML multiplier is formulated by using MCML full adders. In MCML full adder, logic gates are performed based on the six input signals. In MCML multiplier design, the constant current source is used for reducing design complexity as well as for achieving better energy consumption. The MCML multiplier design is shown in Fig. 1.

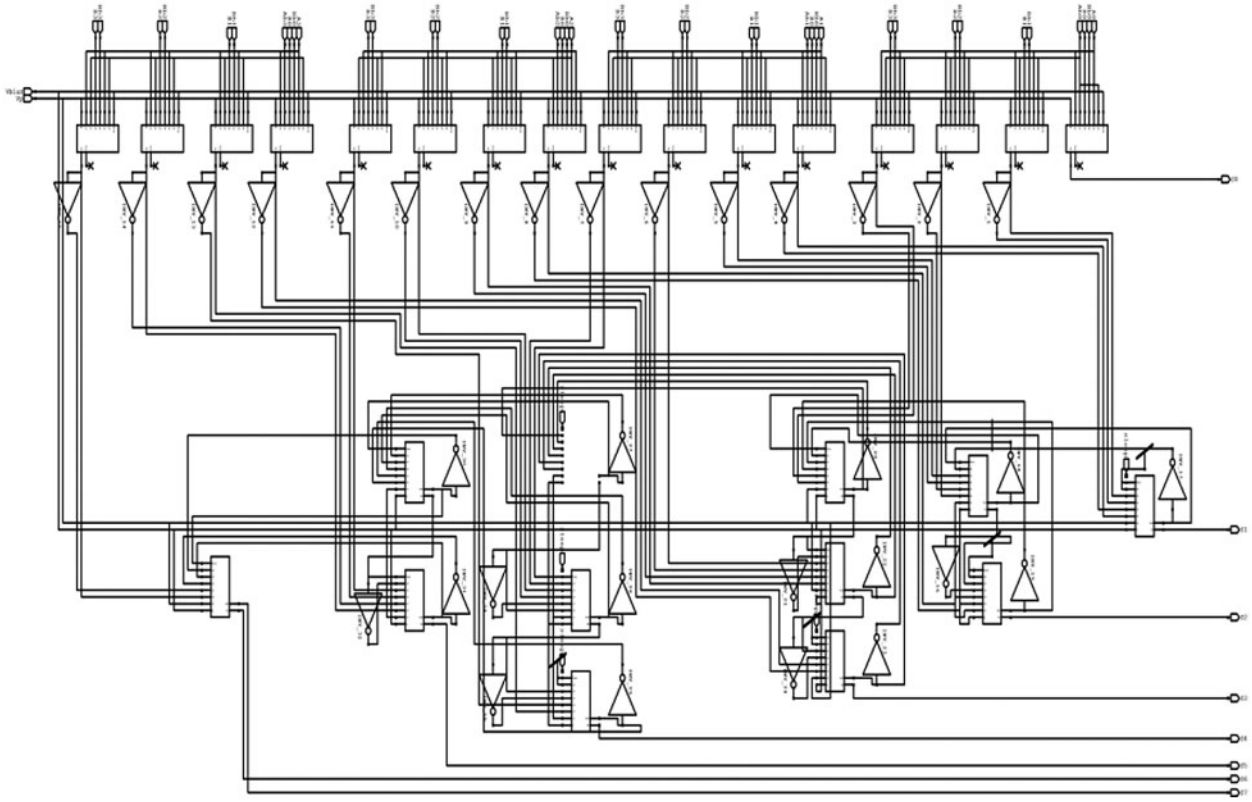

Figure 1: Multiplier design using MCML logic

2.2 Reversible MCML Based Multiplier

The reversible MCML multiplier is designed by using reversible logic based full adder. For minimizing power dissipation and area, proposed research work uses reversible logic based full adder.

Reversible Logic Based Full Adder

Reversible logic is used for enhancing the significance of MCML full adder and by this logic, garbage output and gate counts are evaluated. According to six input signals, operation of logic gates is performed in the MCML full adder. In logic gates, changes have been carried out to achieve reversibility. In reversible gate, the input and output's counts are equal. A one to one mapping is observed between output and input vectors. Using output vector's states, input vector's states can be reconstructed uniquely.

The MCML full adder based on reversible logic is shown in Fig. 2 [17]. One PMOS and nineteen NMOS are used in this proposed design. Outputs are derived according to the inputs. To perform the reversibility, fourth input is maintained as a constant in this circuit (D = 0). P represents the carry and Q represents the full adder sum. Output S and R is similar to input D and C. When compared with the available design of MCML full adder design, very less gate counts are required in proposed MCML full adder.

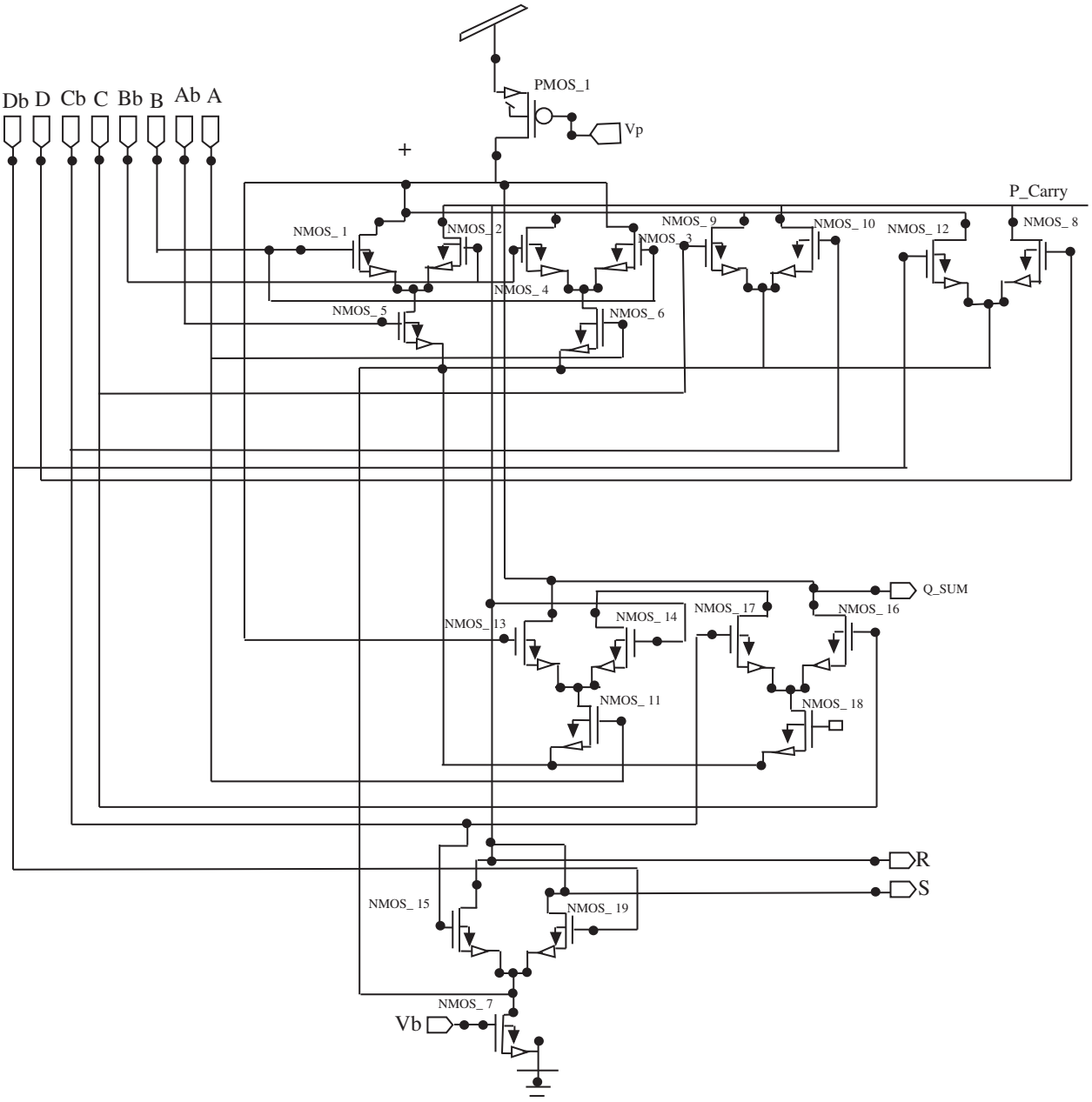

Figure 2: Schematic diagram of reversible logic based full adder

Reversible MCML Multiplier

The full adder is the significant component of reversible MCML multiplier. The reversible MCML multiplier is formulated using reversible logic based full adder. The reversible MCML multiplier achieves better performance due to its capability to retrieve the input data from output and minimizes heat dissipation and area. The schematic diagram of reversible MCML multiplier is shown in Fig. 3.

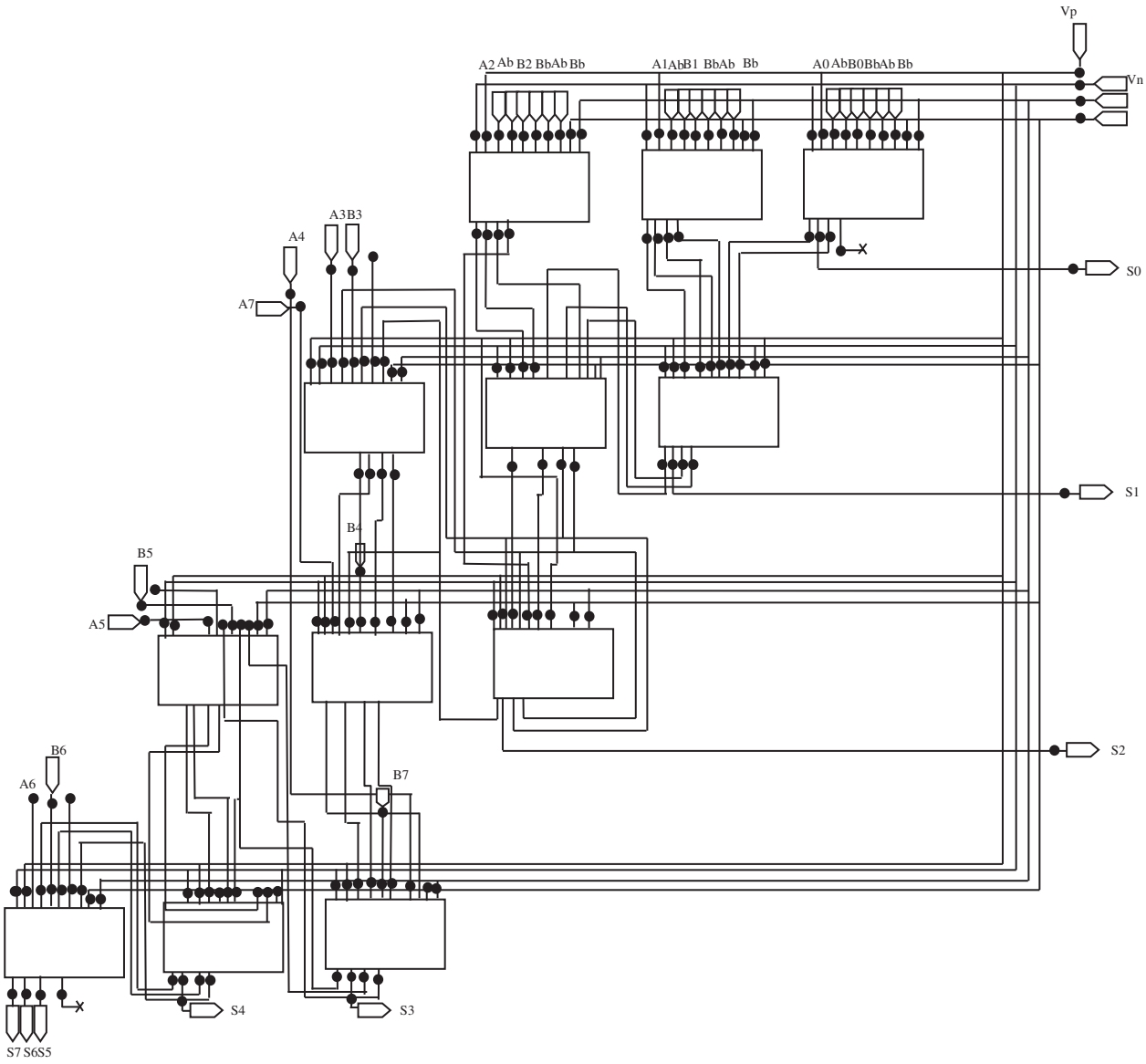

Figure 3: Schematic diagram of the reversible MCML multiplier

2.3 MCML Based D Flip-Flop

Flip flops are the basic tools to store digital data [18,19]. One bit of information can be stored in one flip-flop [20]. It is also utilized as data processor and memory storage elements.

There is an input D (data), input clock and outputs called Q and Q' (inverse of Q) in basic D flip-flop. Fig. 4 shows the pictorial representation of D flip-flop. According to the input, there will be change in output, which is summarized in Tab. 1. The point to be noted is that, these changes is controlled by clock signal.

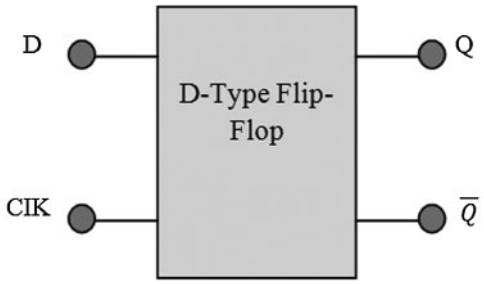

Figure 4: Pictorial representation of D-type flip-flop

Table 1: D flip-flop truth table

Clock	D	Q	Q′
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

The D type flip-flop is designed by using MCML. The operation of MCML D flip-flop is equivalent to the traditional D flip-flop. The conventional D flip-flop is implemented using CMOS technologies. The MCML D flip-flop is implemented using MCML technology to achieve area and power improvements. In MCML based D flip-flop circuit, two PMOS and seven NMOS transistors are used. And also clock is given as an additional input. Based on the clock and input D, the output is produced. Fig. 5 illustrates the circuit of MCML D flip-flop.

2.4 Reversible MCML Based DFF

For minimizing power and area in MCML circuit, implemented the reversible logic in this proposed research work. Based on reversible MCML, the D flip-flop is designed. In this condition, huge power dissipation can be minimized using reversible logic in an effective manner. There are k number of output and k number of inputs in reversible logic design. These are benefits of reversible circuit over combinational circuits and it makes highly an effective one. The reversible MCML D flip-flop design is shown in Fig. 6.

The two PMOS and seven NMOS transistors are used in this proposed design. Outputs are derived based on inputs. After storing desired data, data input is isolated from flip flop's latching circuitry using an additional input called "CLOCK" or "ENABLE" input. With the active clock input, D input condition is copied to output Q due to this. According to the input, there will be change in output.

2.5 MCML Based 8-Bit Register

The registers are synchronous circuits [21,22]. It is extensively used in almost all the applications to store the state information. An n-bit register has n flip-flops which are capable to store n bit binary information. A common clock is used for each flip-flop in the register. In this proposed

work, MCML based flip-flops are combined to form a MCML based register. The schematic diagram of MCML based register is shown in Fig. 7.

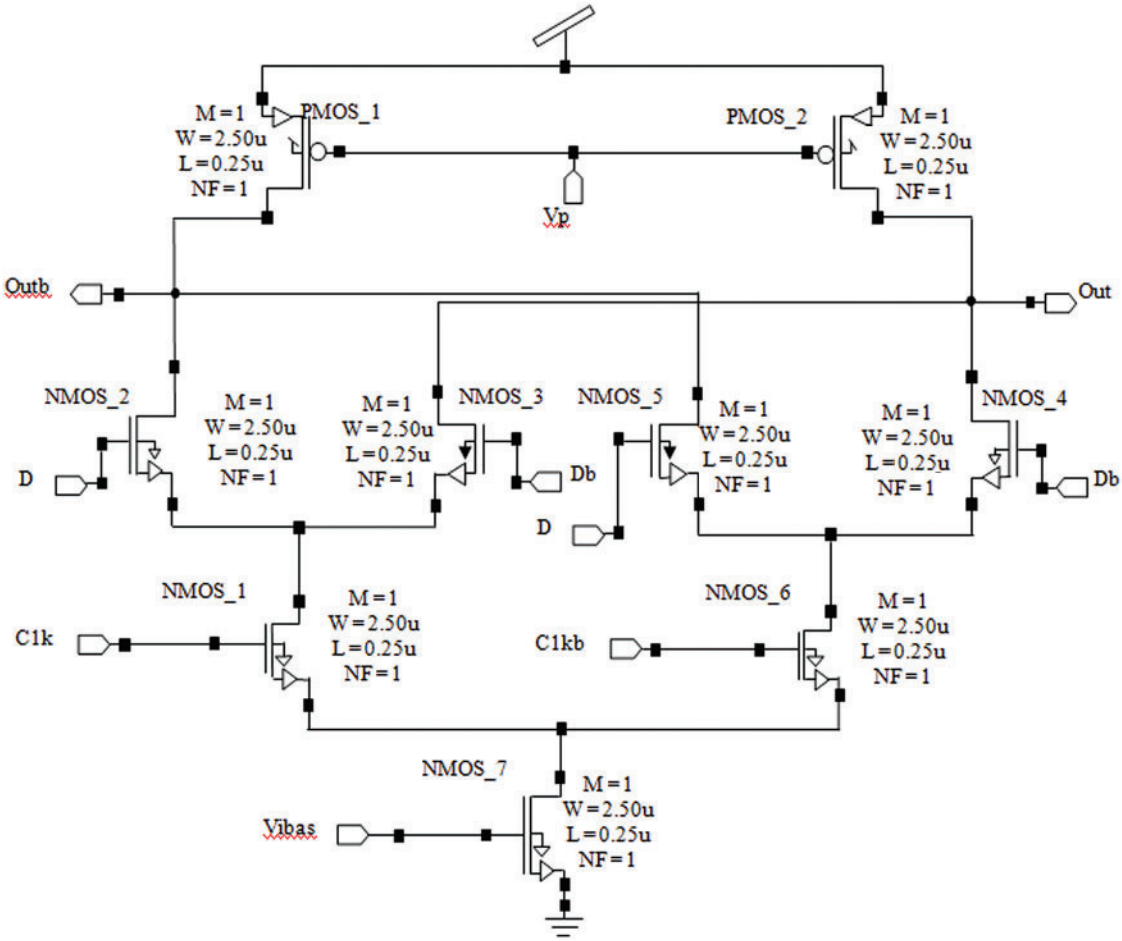

Figure 5: MCML based D flip-flop circuit

2.6 Reversible MCML Based 8-Bit Register

In this proposed research work, 8-bit register is designed for ultralow power design. The group of reversible MCML based flip-flops is combined to form a register. The schematic diagram of reversible MCML based register is shown in Fig. 8.

The 8-bit register holds an 8-bit logical value (i.e., 10110110), and it is formed by a collection of eight reversible MCML D flip-flops. In order to form a register from a collection of reversible MCML D flip-flops, the reversible MCML flip-flops must all run on the same clock signal.

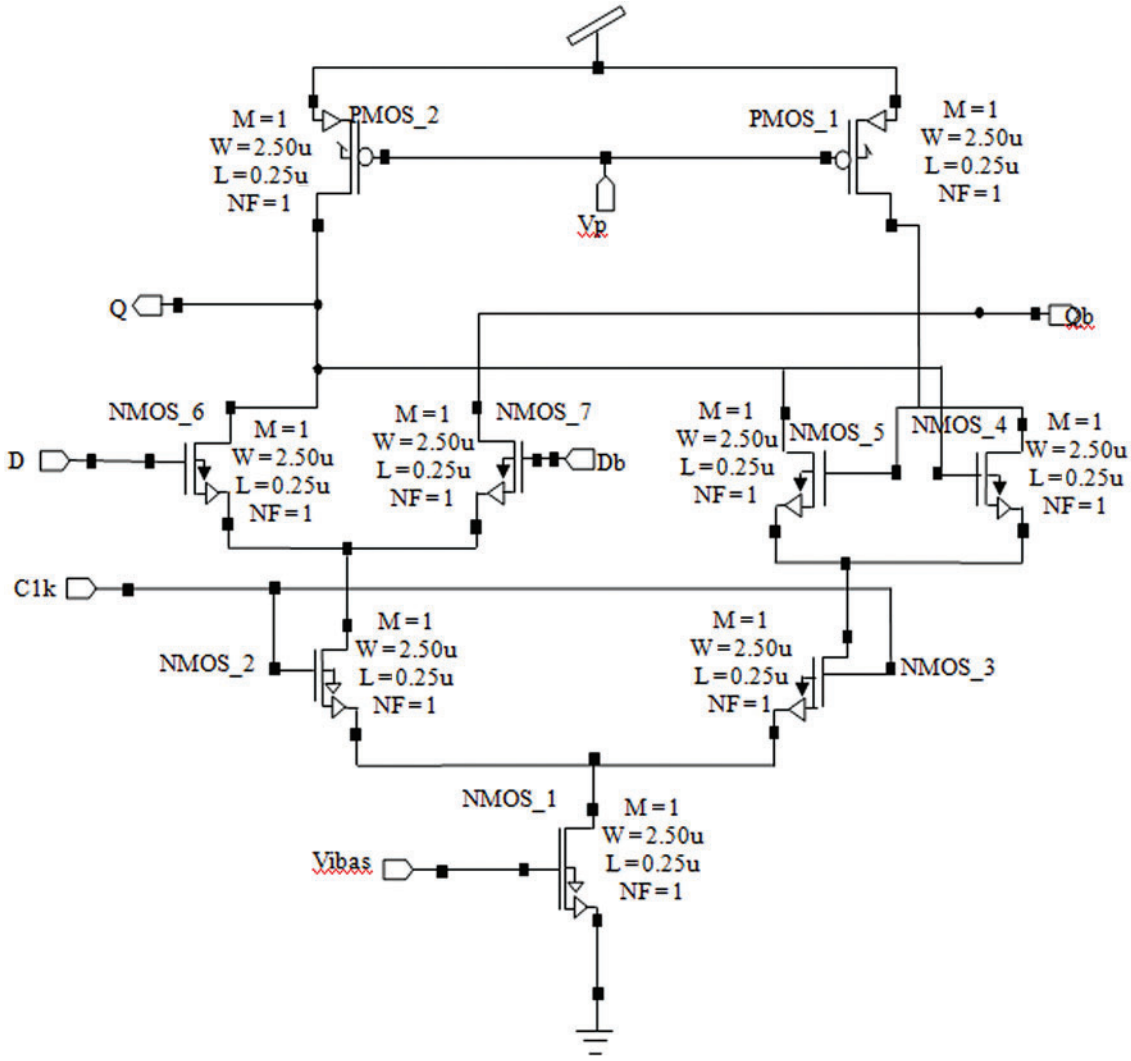

Figure 6: Reversible MCML based DFF

3 Results & Discussion

The MCML multiplier, Reversible MCML multiplier, MCML based DFF, Reversible MCML based DFF, MCML based 8-bit register and Reversible MCML based 8-bit register are implemented using Tanner EDA tool at 180 nm technology. The performance is analyzed in terms of static power dissipation, average power, static current and area. The simulation output of Reversible MCML based multiplier and Reversible MCML DFF circuits are shown in Figs. 9 and 10 respectively.

The simulation output of the reversible MCML based register is shown in Fig. 11. Tab. 2 summarizes the evaluation of the results of proposed Reversible MCML approach.

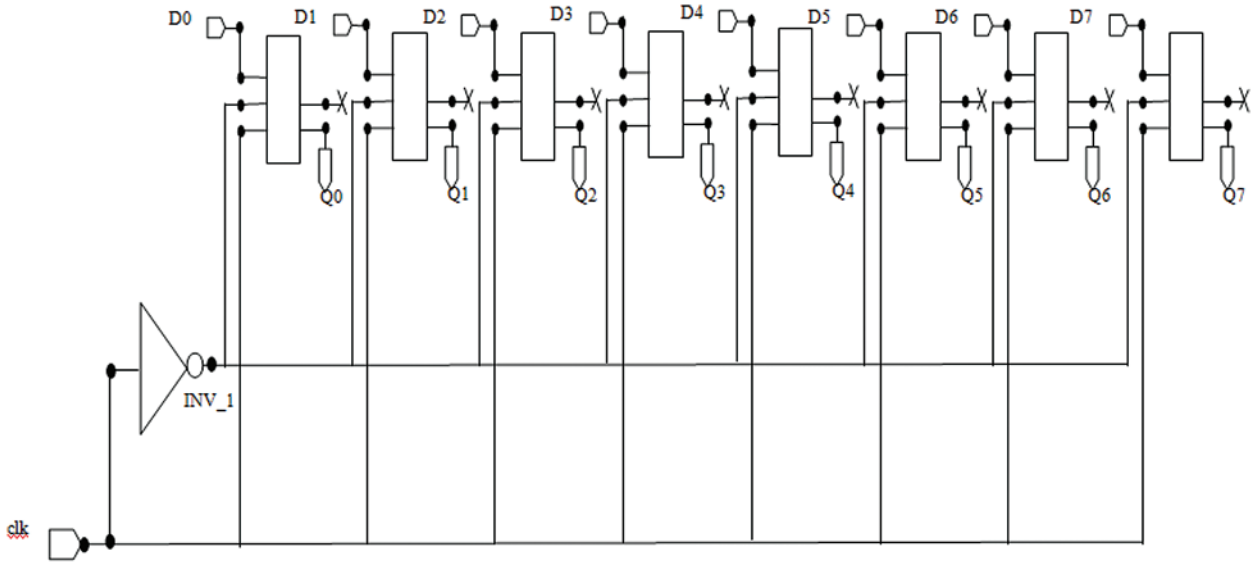

Figure 7: Schematic diagram of MCML based register

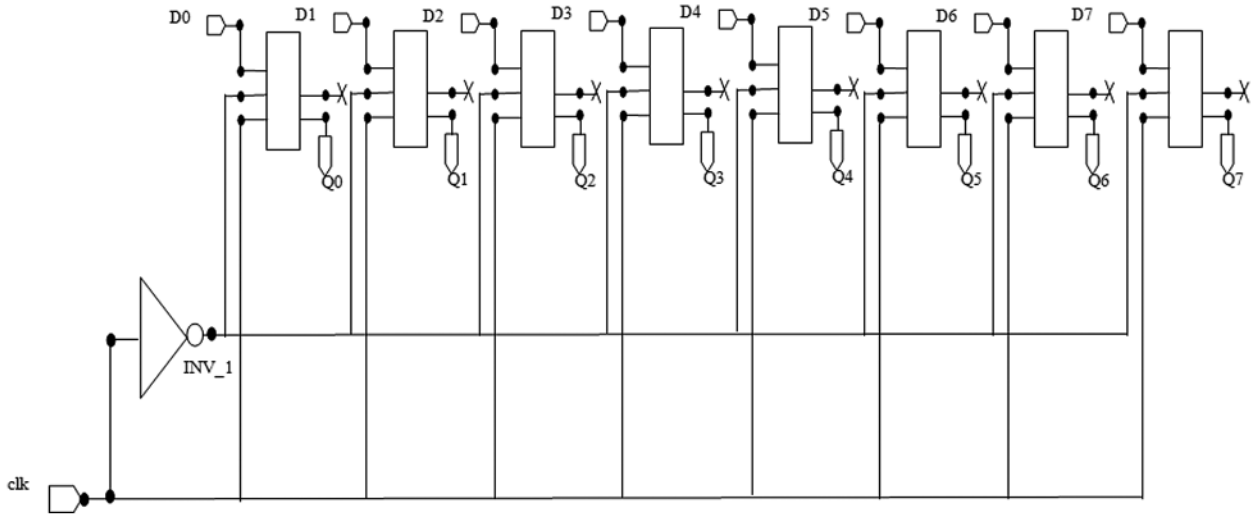

Figure 8: Schematic diagram of reversible MCML based register

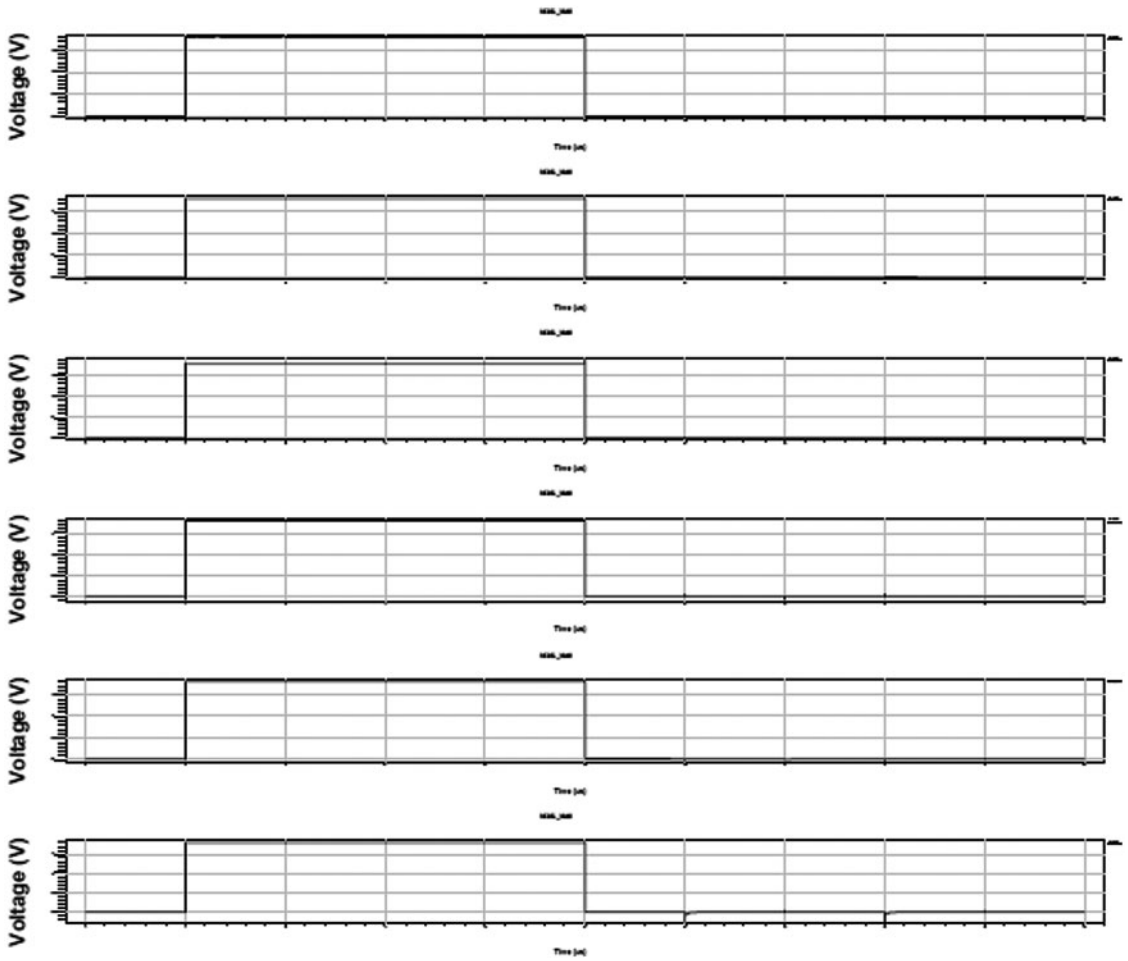

Figure 9: Simulation output of reversible MCML based multiplier

Fig. 12 shows the average power of MCML based multiplier, Reversible MCML based multiplier, MCML based DFF, Reversible MCML based DFF, MCML based 8 bit register and Reversible MCML based 8-bit register. In this proposed work, the reversible logic based circuits achieves minimum average power consumption due to its capability to retrieve the input data from output. The proposed reversible MCML multiplier attains 0.683 mW whereas MCML based multiplier achieves 6.19 mW. Average power of the Reversible MCML based DFF is 0.56μW when MCML based DFF attains 5.31 μW. The Reversible MCML based 8-bit register attains 04.04 μW whereas MCML based 8-bit register 8.29 μW.

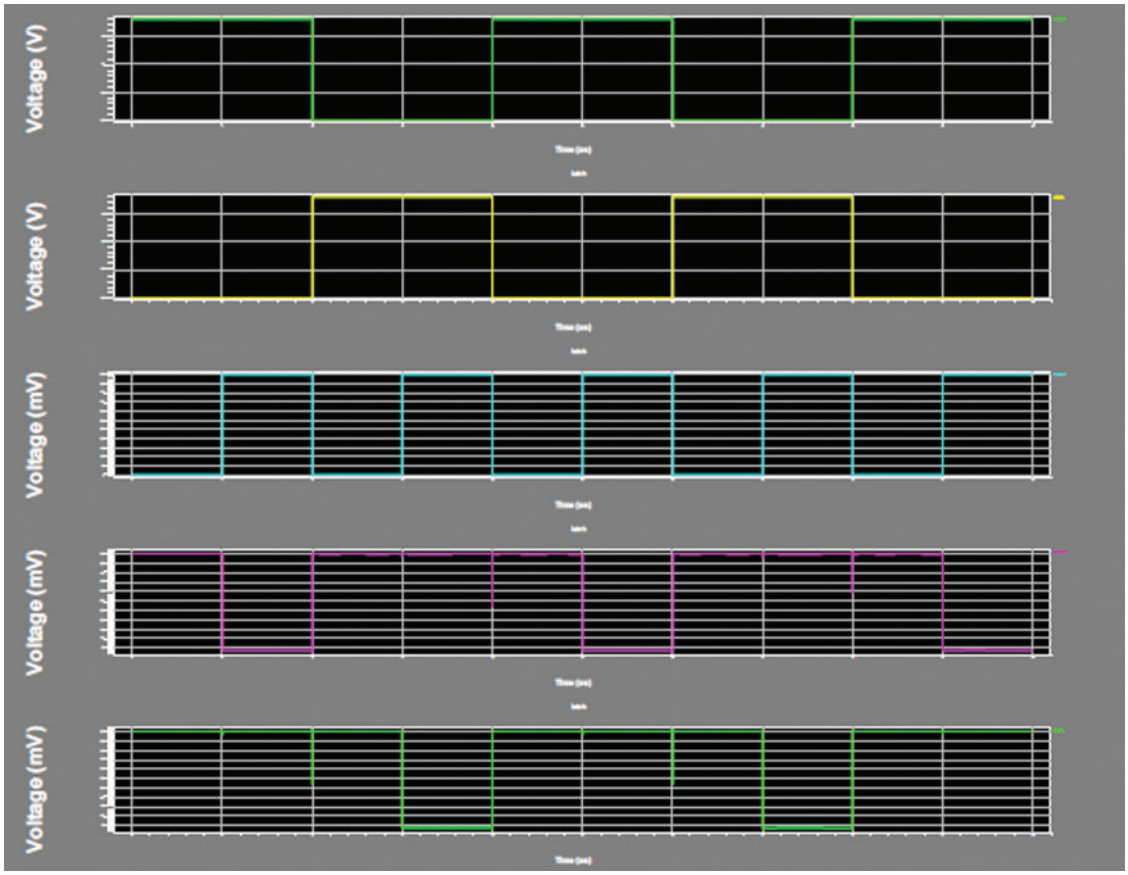

Figure 10: Simulation outputof reversible MCML based DFF

In Fig. 13, MCML based multiplier, Reversible MCML based multiplier, MCML based DFF, Reversible MCML based DFF, MCML based 8-bit register and Reversible MCML based 8-bit register are analyzed with respect to static power dissipation.

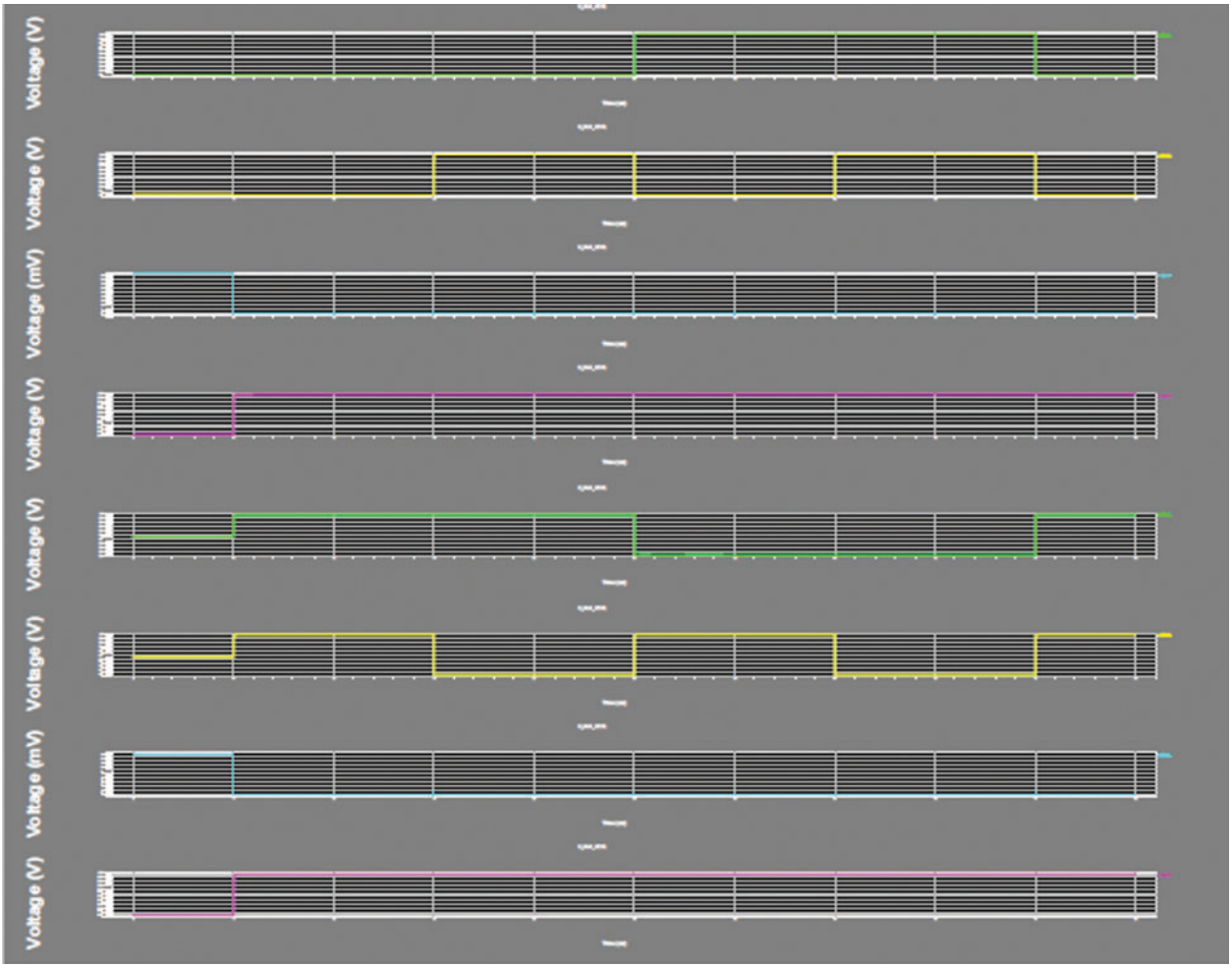

Figure 11: Simulation output of reversible MCML based register

Table 2: Performance comparison

Parameter	Multiplier		DFF		8-bit register	
	MCML	Reversible MCML	MCML	Reversible MCML	MCML	Reversible MCML
Average power	6.19 mW	0.683 mW	5.312 μW	0.5678 μW	8.2939 μW	04.049 μW
Static power dissipation	183.2 nW	97.2 nW	4.89 μW	1.251 μW	11.854 μW	1.1928 μW
Static current	101.7 nA	54 nA	2.71 μA	0.69 μA	6.585 μA	0.662 μA
Area (no. of transistors)	458	240	22	18	178	144

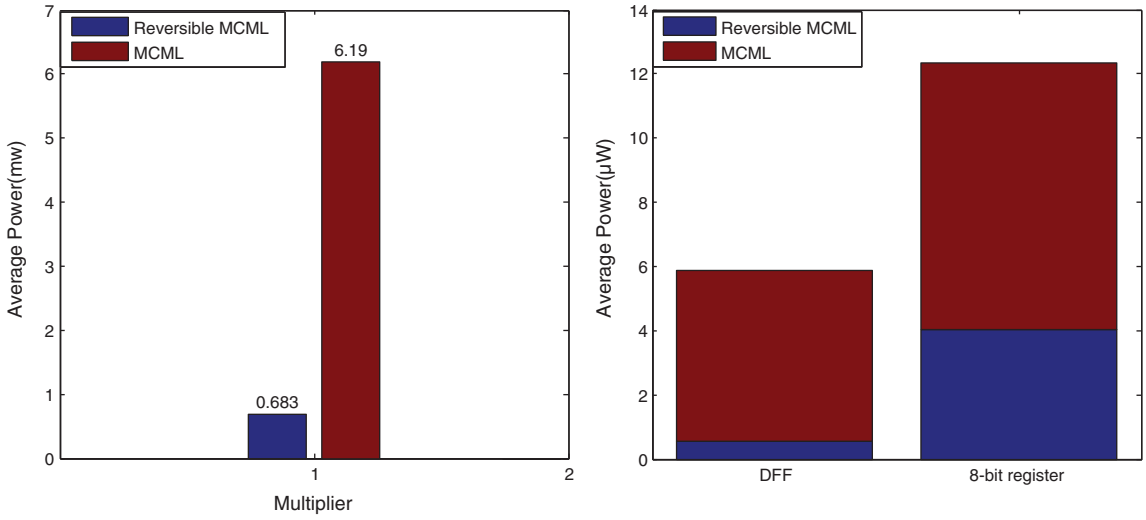

Figure 12: Average power consumption

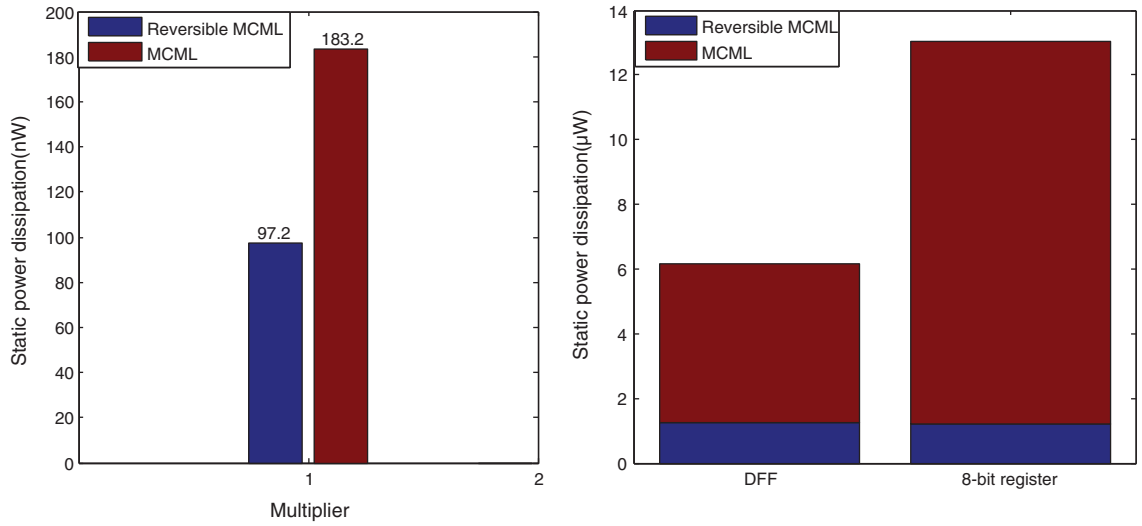

Figure 13: Comparison for static power dissipation

The proposed Reversible MCML multiplier attains 97.2 nW of static power dissipation whereas MCML multiplier achieves 183.2 nW. The Reversible MCML based DFF's static power dissipation is 1.25 μW when MCML based DFF attains 4.89 μW. The Reversible MCML based 8-bit register attains 1.19 μW whereas MCML based 8-bit register provides 11.85 μW.

The static current comparison of the MCML based multiplier, Reversible MCML based multiplier, MCML based DFF, Reversible MCML based DFF, MCML based 8-bit register and Reversible MCML based 8-bit register are shown in Fig. 14. The proposed reversible MCML multiplier attains 54 nA of static current whereas MCML based multiplier achieves101.7 nA. The static current of the Reversible MCML based DFF is 0.69 μA when MCML based DFF attains 2.71 μA. The Reversible MCML based 8-bit register attains 0.66 μA whereas MCML based 8-

bit register achieves 6.58 μA. The experimental results show that the proposed reversible MCML achieves minimum static current than conventional MCML.

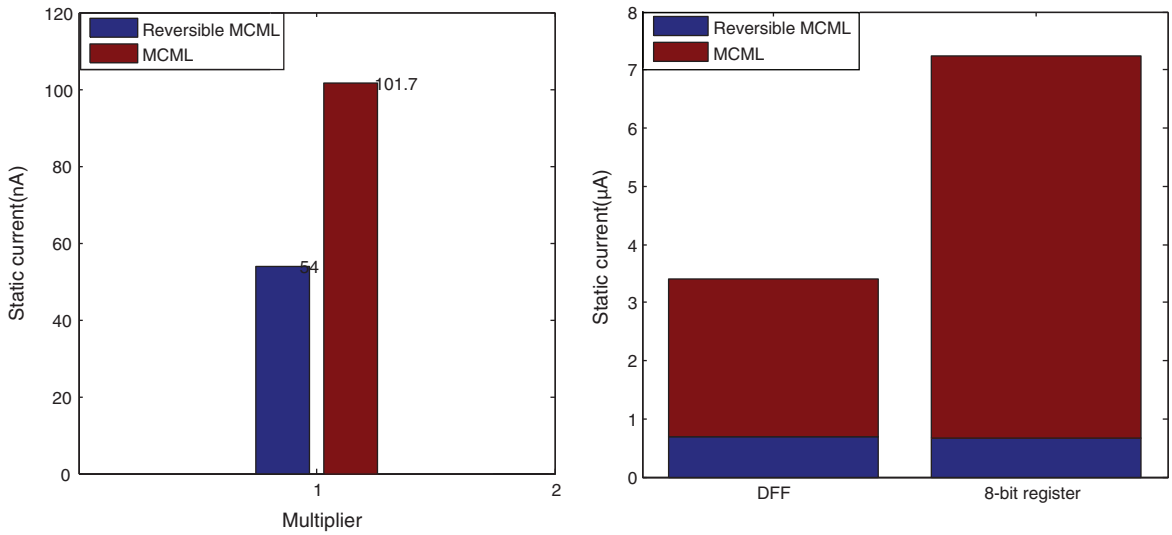

Figure 14: Comparison of static current

Area of the MCML based multiplier, Reversible MCML based multiplier, MCML based DFF, Reversible MCML based DFF, MCML based 8-bit register and Reversible MCML based 8-bit register are shown in Fig. 15. In this proposed work, area is reduced due to the function of reversibility. The proposed Reversible MCML has area of 240 whereas MCML multiplier has 458. Area of the Reversible MCML based DFF is 18 whereas MCML based DFF has 22. The Reversible MCML based 8-bit register has 144 whereas MCML based 8-bit register has 178. As shown in experimental results, the proposed reversible MCML achieves minimum area compared with MCML.

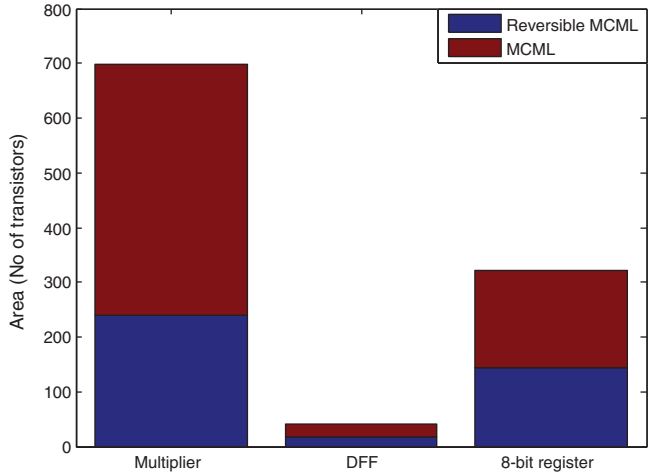

Figure 15: Area comparison

4 Conclusion

In this proposed research work, multiplier based on reversible MCML, reversible MCML based flip-flop and reversible MCML based register circuits are designed to achieve better area and power. The reversible logic is being used very fast because of its ability in designing a highly complex circuit with minimized power dissipation. The proposed circuit is implemented using Tanner EDA tool at 180 nm technology. From simulation outcome, it is be concluded that the area of proposed reversible MCML based multiplier is 240 which is 47.59% lower than MCML based multiplier, reversible MCML based flip-flop achieves 18.18% of area reduction than MCML based DFF and reversible MCML based register attains 19.10% of area reduction than MCML based register. The performance of the MCML multiplier, Reversible MCML multiplier, MCML based DFF, Reversible MCML based DFF, MCML based 8-bit register and Reversible MCML based 8-bit register are evaluated in terms of static current, static power dissipation, average power and area. In future, reversible logic is applied in C-slow processor with FIFO memory. Here, the performance of processors is enhanced by exploiting multithreading technique in single core processors.

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