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Article

Performance Enhancement of PV Based Boost Cascaded Fifteen Level Inverter for AC Loads

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Abstract: In this research work, single-stage fifteen levels cascaded DC-interface converter (CDDCLC) is proposed for sun arranged photovoltaic technology (PV) applications. The proposed geography is joined with help DC chopper and H-associate inverter to upgrade the power converter to accomplish the diminished harmonic profile. In assessment with the customary inverter structures, the proposed system is used with diminished voltage stress, decreased switch count and DC source tally. The proposed research work with cascaded DC link converter design requires three DC sources for combining fifteen-level AC output. This investigation structure switching technique is phase opposition and disposition pulse width modulation technique (POPD) which results in improved quality of obtained output AC power with 6.73% THD and also determinedly recommended for power converters used in UPS and drive applications since it is extremely affordable. A simulation and prototype model of fifteen-level CDDCLC system is deployed and its performance is analyzed for various operating conditions.

Keywords: Cascaded DC link converter (CDDCLC); modified phase opposition and disposition (MPOPD PWM); photovoltaic (PV); DC interface boost converter

1 Introduction

The new type of power converter options for high-power functions appear in multilevel inverters (MLIs) in power converters, particularly for sustainable power source combinations and uninterruptible power supplies [1,2]. MLI's traditional multilevel inverter topologies are flying capacitor MLI (FCMLI), diode clamped MLI and cascaded multilevel inverter CMLI [3,4]. Each topology has its advantages and limitations. CMLI synthesizes the AC voltage waveform of the staircase from a few DC sources among the setup with decreased consonant substance [5]. So the configuration of CMLI is more desirable than the other two configurations.

In order to achieve the nominal output voltage in CMLI, [6,7], a step-up dc-dc converter is connected between DC sources and H-bridges. In view of the quantity of regulated force switches and DC sources, the feasibility of the CMLI and lift CMLI (BCMLI) configurations [8] is compromised.

Some modifications can be made in the standard CMLI and BCMLI frameworks [9–12] in this process. CMLI with decreased switch count is proposed in this framework. In addition, it is shown that the ostensible yield voltage is obtained by presenting the raise chopper circuit between the DC sources and the DC-interface inverter.

The Boost Chopper Network raises the DC input voltage to the nominal voltage level. This results in the number of DC sources and power switches being decreased. In this paper, for UPS applications, a single-phase fifteen-level asymmetrical source boost DC-link CMLI (BDCLCMLI) system is developed. For DC-link switches [13–21], a multicarrier sinusoidal pulse-width modulation (MCSPWM) switching strategy has been developed to obtain a better quality of AC power with an improved harmonic profile.

For each H-bridge and m-level inverter, a separate DC bus is needed; 2 (m−1) numbers of switches per step and 2 (m−1) numbers of ant parallel diodes are required. Topology of seven level cascaded multilevel inverter with RL load is shown in Fig. 1.

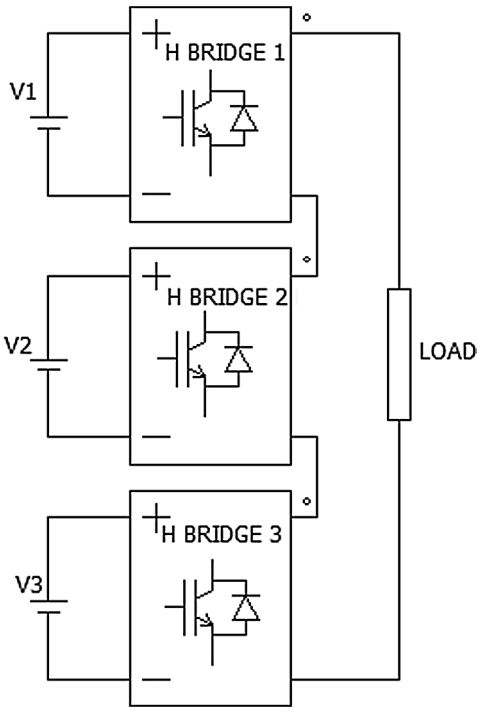

Figure 1: Cascaded multilevel inverter (Seven-level)

A single-phase seven-level asymmetrical source boost converter in deployed in this work. [Uthirasamy et al. (2014)]. The BDCLCMLI (DC-link CMLI) framework is optimized for UPS Applications. The general structure of the BDCLCMLI seven level scheme is shown in Fig. 2. For DC-link switches, multicarrier sinusoidal pulse-width modulation (MCSPWM) switching strategy is built to obtain better quality of AC power (with reduced harmonic content). Circuit diagram of fifteen levels Boost DC-link which is cascaded with multilevel inverter is given in Fig. 3.

The dc/dc converter extricates the greatest power from the dc-interface to the PV series. [Ajami et al. (2013)]. It should be noted that the immediate association of the PV string to the dc-connect, due to the second consonant swaying of the dc-interface, results in a wavering of the PV string's extricated power.

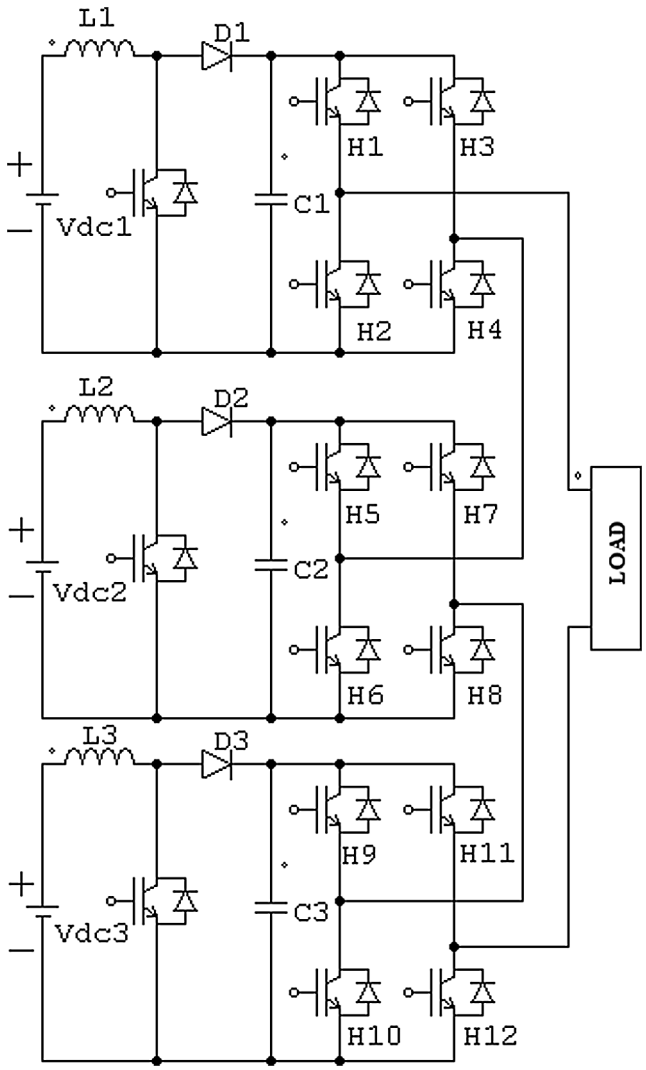

Figure 2: Boost cascaded multilevel inverter (Seven levels)

2 Configuration of BDCLCMLI System

Three lopsided DC voltage sources, support chopper unit, DC-connect module (DCLM) and a typical H-connect inverter establish a BDCLCMLI framework. Further, in corresponding to the DC-interface framework H-connect inverter is associated. The BDCLCMLI configuration withholds various numbers of levels and switches which is calculated by Eqs. (1) and (2),

$$N_{level} = 2^{(n+1)} - 1 \tag{1}$$

$$N_{switch} = 2r + 4p \tag{2}$$

where,

N_{level}- number of levels,

N_{Switch}-number of switches in BDCLCMLI,

n- Number of boost chopper units.

r- Number of DC source count.

p-Number of H-bridge inverter count.

The proposed topology consists of two parts, they are

i. Boost chopper with Solar input
ii. Level generation unit with Common H bridge

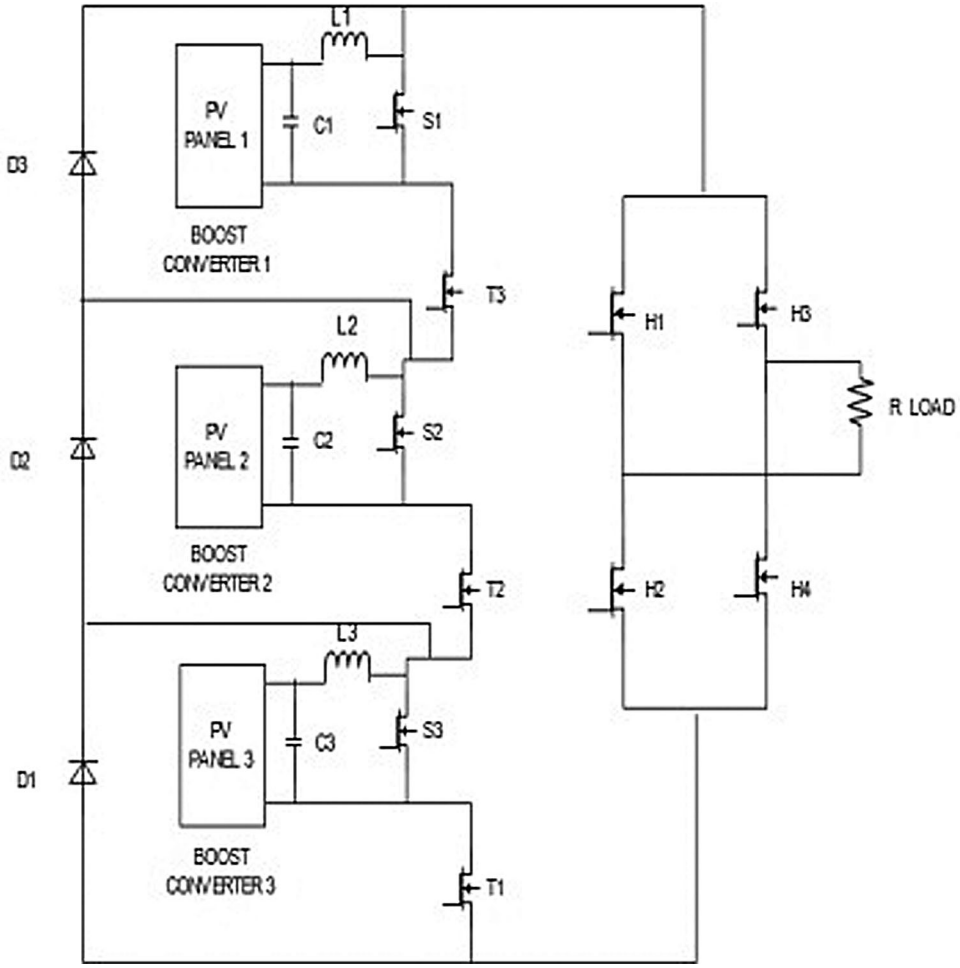

Figure 3: Circuit diagram of fifteen levels boost DC-link cascaded multilevel inverter

2.1 Boost Chopper with Solar Input

The asymmetrical DC source output voltage is always unidirectional. And each boost chopper unit is connected with asymmetrical DC sources.

Fig. 4 represents the structure of the boost chopper. Believing the framework to be lossless, the normal yield voltage of each lift chopper is gotten using Eq. (3)

$$V_{on} = \frac{V_{dcn}}{1 - K_n} \tag{3}$$

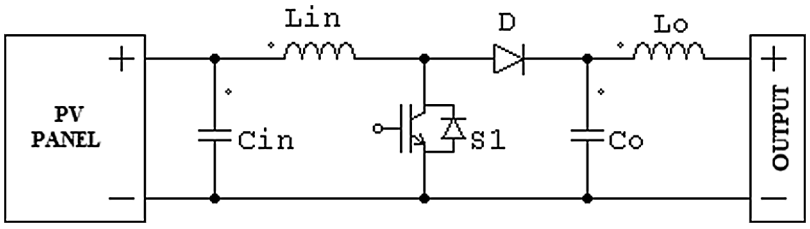

Figure 4: Boost chopper

2.2 Level Generation Unit with Common H Bridge

The proposed asymmetrical multilevel inverter is made up of two parts. They are the Level generation unit and common H Bridge. The boost chopper output voltage of isolated sources is switched via the level generation unit to produce the desired fifteen levels. The switching states are listed in Tab. 1. The asymmetrical topology produces fifteen levels when compared to the symmetrical one whereas the conventional topology produces only seven levels. Hence the topology saves the number of switches and sources.

Table 1: Switching states

Level	T1	T2	T3	H1	H2	H3	H4	Output voltage (Vo)
0	0	0	0	1	0	0	1	0
1	1	0	0	1	0	0	1	V_1
2	0	1	0	1	0	0	1	V_2
3	1	1	0	1	0	0	1	(V_1+V_2)
4	0	0	1	1	0	0	1	V_3
5	1	0	1	1	0	0	1	(V_1+V_3)
6	0	1	1	1	0	0	1	(V_2+V_3)
7	1	1	1	1	0	0	1	$(V_1+V_2+V_3)$
0	0	0	0	0	1	1	0	0
−1	1	0	0	0	1	1	0	$-V_1$
−2	0	1	0	0	1	1	0	$-V_2$
−3	1	1	0	0	1	1	0	$-(V_1+V_2)$
−4	0	0	1	0	1	1	0	$-V_3$
−5	1	0	1	0	1	1	0	$-(V_1+V_3)$
−6	0	1	1	0	1	1	0	$-(V_2+V_3)$
−7	1	1	1	0	1	1	0	$-(V_1+V_2+V_3)$

The level generation unit having sub-modules can produce only unidirectional voltage. So a common H bridge is used to reverse the generated voltage. This in turn helps to produce bipolar symmetrical waveform and reduces the individual H bridge at the same time. The switches in the level generation unit are marked as T1, T2 and T3. The common H bridges marked as H1, H2, H3 and H4.

3 Operating Modes

The proposed system is switched under nine states to obtain fifteen-level. The ac output voltage level is controlled through multi carrier PWM. The operation of level generation unit is explained from Mode 1 to Mode 8 as shown in Figs. 5a–5h. The reverse voltage technique is explained through Mode 9 in Fig. 5i.

The lift chopper switch S_b is turned ON at $t = T_{ON2}$ and current which flows through inductor L2 varies linearly from I_3 to I_4

Hence, the voltage across inductor L2 is derived as

$$\mathrm{Vd}\ \ 2 = \mathrm{L2}\ \ \frac{I4 - I3}{Ton2} \tag{4}$$

Now, vitality contribution to inductor L2 from the source

$$E_{i2} = Vd_{2.}\, Is_{2.} T_{ON2} \tag{5}$$

At $t = T_{OFF2}$ the lift chopper switch S_b is switched OFF and current through the inductor L_2 flows linearly from I_4 to $I_{3.}$

Average output voltage of boost chopper II is obtained

$$V_{obc2} = V_{dc2} + L_2 \frac{\mathrm{dIs2}}{\mathrm{Toff2}} \tag{6}$$

During this time, the energy which is released by the inductor L_2 to B_{DCIM} is given by,

$$E_{o2} = (V_{obc2} - V_{d2}) I_{s2}.\ T_{OFF2} \tag{7}$$

The change in voltage over the capacitor C2 is derived by

$$\Delta e_{c2} = I_{o2} * \left[\frac{V_{obc2\ -L2(l4-I3)}}{V_{obc1} * f * C2} \right] \tag{8}$$

Voltage across the inductor 4 is derived as

$$V_{d1} = L_1 \frac{I2 - I1}{\mathrm{Ton1}} \tag{9}$$

The vitality contribution to inductor 4 from source Vd1 is identified as

$$E_{i1} = V_{d1} I_1 T_{ON1} \tag{10}$$

At $t = T_{OFF1}$ lift chopper switch *Sa* is switched OFF and the current which flows through inductor 4 falls linearly from I_2 to I_1.

At $t = T_{OFF1}$ lift chopper switch Sa is switched OFF and the current through the inductor 4 falls linearly from I_2 to I_1

The normal yield voltage of lift chopper I can be expressed as

$$V_{obc1} = V_{d1} + 4 \frac{\mathrm{dIs1}}{\mathrm{Toff1}} \tag{11}$$

At this moment the energy which is released by inductor L1 to the BDCLM is given by

$$E_{o1} = (V_{obc1} V_{d1}) I_{s1}.T_{OFF1} \tag{12}$$

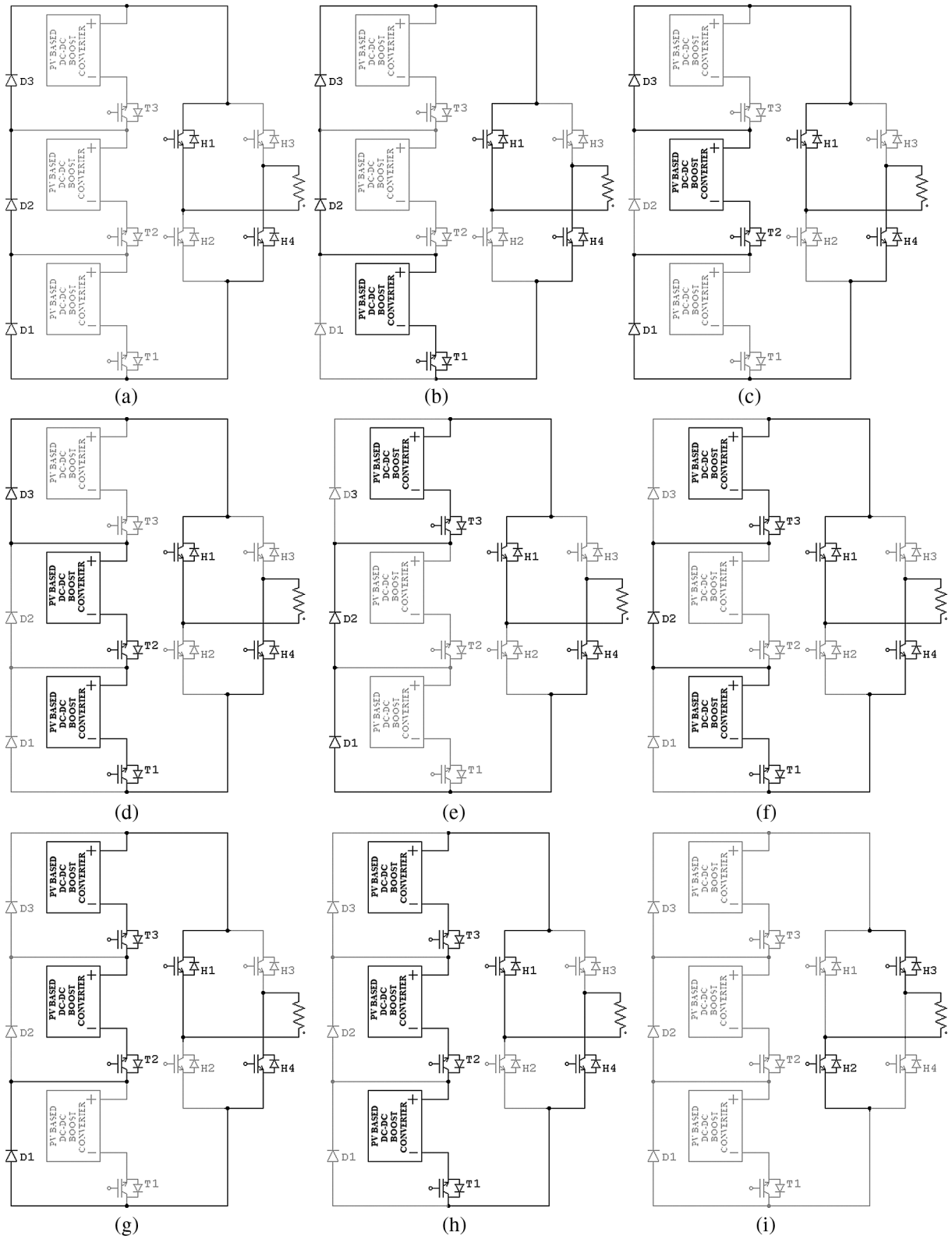

Figure 5: (a) Mode 1 ($V_0 = 0$ V) (b) Mode 2 ($V_0 = 1$ V) (c) Mode 3 ($V_0 = 2$ V) (d) Mode 4 ($V_0 = 3$ V) (e) Mode 5 ($V_0 = 4$ V) (f) Mode 6 ($V_0 = 5$ V) (g) Mode 7 ($V_0 = 6$ V) (h) Mode 8 ($V_0 = 7$ V) (i) Mode 9 ($V_0 = -V$)

The ripple in the inductor current can be obtained as

$$\Delta i1 = \frac{V_{d1} - Vobc_1}{LfVd1} Vobc1 \tag{13}$$

The adjustment in voltage overCapacitor t1 can be written as

$$\Delta e_{c1} = I_{o1} * \frac{V_{ob1} - L_1(I_{2-I_1})}{V_{ob1} * f * C_1} \tag{14}$$

At t = TON3 boost chopper switch S_a and S_b are turned ON and current through the inductors L_1 and L_2 increases gradually from I_1 to I_2 and I_3 to I_4 respectively.

At right now, vitality contribution to inductor L_1 from source V_{d1} and energy fed to the inductor L_2 from source Vd_2 are

$$E_{i3} = (V_{d1} + V_{d2}).\ (I_{s1} + I_{s2}) \tag{15}$$

Boost chopper switches S_a and S_b are switched OFF and current through inductor L_1 and L_2 drops linearly from I_2 to I_1 and from I_4 to I_3.

At this moment the energy discharged from inductor

L_1 and L_2 to B_{DCLM} is given by,

$$E_{o3} = [(V_{obc1} - V_{d1)}I_{s1} + (V_{obc2} - V_{d2})I_{s2}].T_{OFF3} \tag{16}$$

The adjustment in voltageacross capacitor C_1 and C_2 is expressed as

$$\Delta V_{c1+}\Delta V_{c2} = I_{o1} * \left[\frac{V_{o1\ -L1(l2-I1)}}{V_{o1} * f * C1}\right] + I_{o2} * \left[\frac{V_{o2\ -L2(l4-I3)}}{V_{o2} * f * C2}\right] \tag{17}$$

The positive half cycle magnitude of AC output voltage are written as

$$V_{o1} = V_{obc1} \tag{18}$$

$$V_{o2} = V_{obc2} \tag{19}$$

$$V_o = V_{o1+}V_{o2} = V_{obc1} + V_{obc2} \tag{20}$$

The negative half cycle magnitude of AC output voltage are expressed as

$$V_{o1} = -V_{obc1} \tag{21}$$

$$V_{o2} = -V_{obc2} \tag{22}$$

$$V_o = (V_{o1+}V_{o2})_{=} - [V_{obc1} + V_{obc2}] \tag{23}$$

To produce positive or negative seven levels, the switches T1-T3 are operated as per the switching pattern listed in the Tab. 1. The DC-DC boost converter outputs are regulated with the ratio 1:2:4. The H bridge switches are operated as shown in the table to produce the seven level output on both positive and negative sides. Mode 1 –Mode 8 H1& H2 switches are turned ON to produce the positive voltage. Similarly to produce negative output voltage H3&H4 switches are turned ON as shown in Fig. 5i.

4 Modified MCSPWM Switching Technique

PWM techniques are classified corresponding to the switching frequency. Sinusoidal PWM, space-vector PWM and concerned harmonic reduction are created such that it reduces the distortion in MLIs.

These are considered to be the existing modulation techniques. Vertical transporter dispersion and even bearer dissemination are the two broad categories of MCS PWM control methods [2]. Fig. 6 shows the unipolar MCSPWM switching pattern. It is elevated to trigger the DC-connect switches of CDDCLC.

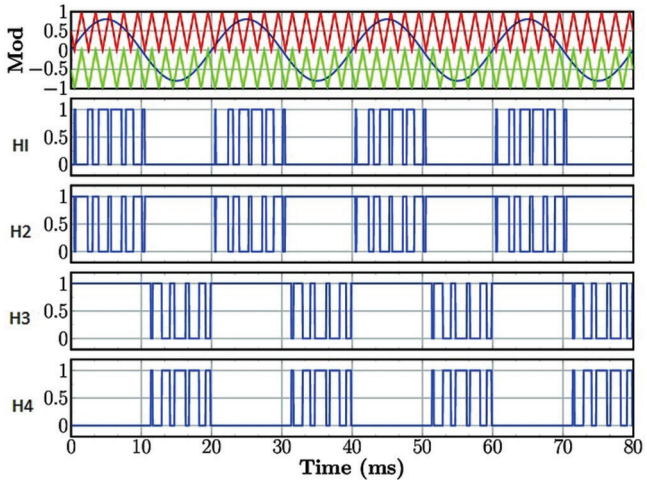

Figure 6: Unipolar POPD PWM

In this proposed work, a unipolar sine and trapezoidal reference with a triangular transporter is utilized to produce terminating beats for a 15 level inverter. For m-level inverter utilizing unipolar multi-bearer systems, (m−1)/2 transporters with a similar recurrence fc and same top to-top plentifulness Ac are utilized. The reference waveform has adequacy Am and recurrence fm and it is put at the zero reference. The reference wave is ceaselessly contrasted and every one of the transporter signals On the off chance that the reference wave is in excess of a bearer signal, at that point the dynamic gadgets comparing to that transporter are turned on.

The proposed PWM is delineated in Figs. 6 and 7. It includes four three-sided transporters and two reference signals (sine wave) for PWM age and the relating simple hardware for base PWM age for each level as depicted in Fig. 7.

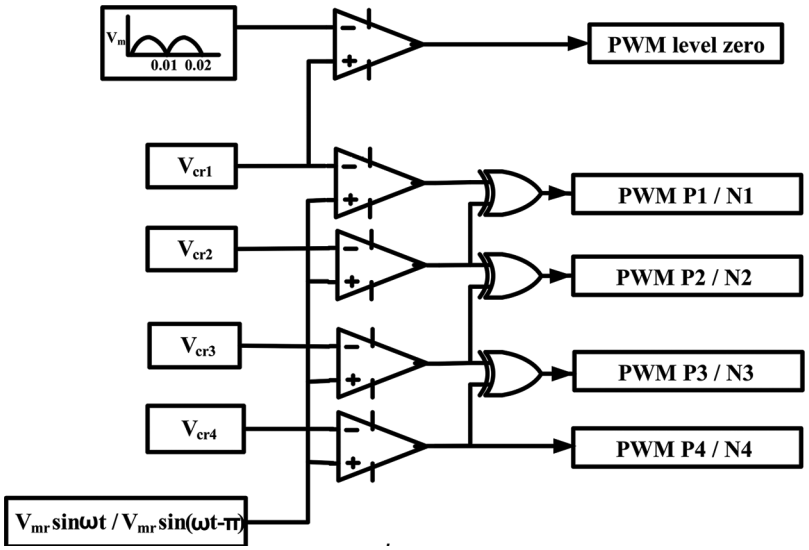

Figure 7: Circuit for PWM generation

The reference wave is consistently contrasted and every one of the transporter signals. On the off chance that the reference wave is in excess of a transporter signal, at that point the dynamic gadgets comparing to that bearer are turned on. Otherwise, the devices are switched off. The frequency of the carrier signal determines the frequency of the AC voltage waveform. And the magnitude of the reference signal determines the effective RMS value of the output voltage waveform.

5 MATLAB Simulation Results

To validate the proposed method, simulation results summarized in this section have been obtained with a single-phase 15-level CDDCLC using MATLAB/Simulinkenvironment as shown in Figs. 8–10. The simulation conditions are shown in Tab. 2.

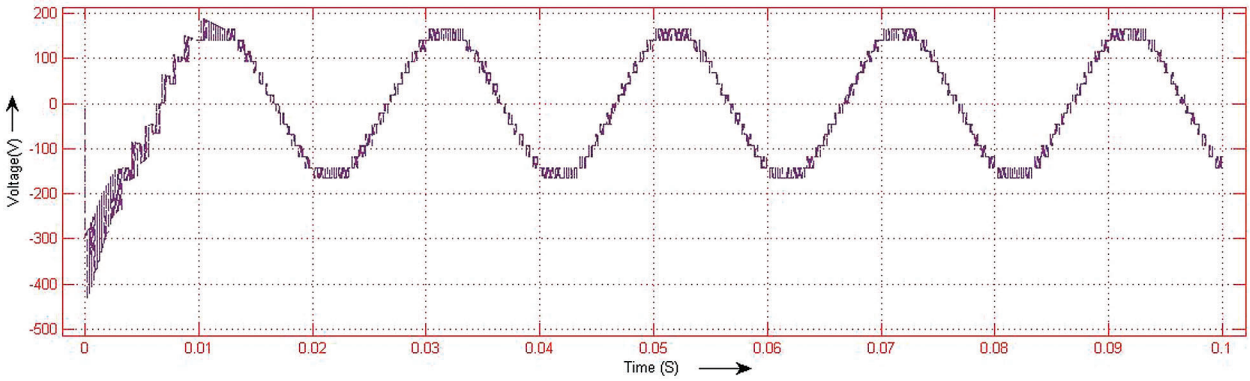

Figure 8: Output (Level generation unit and H bridge) voltage

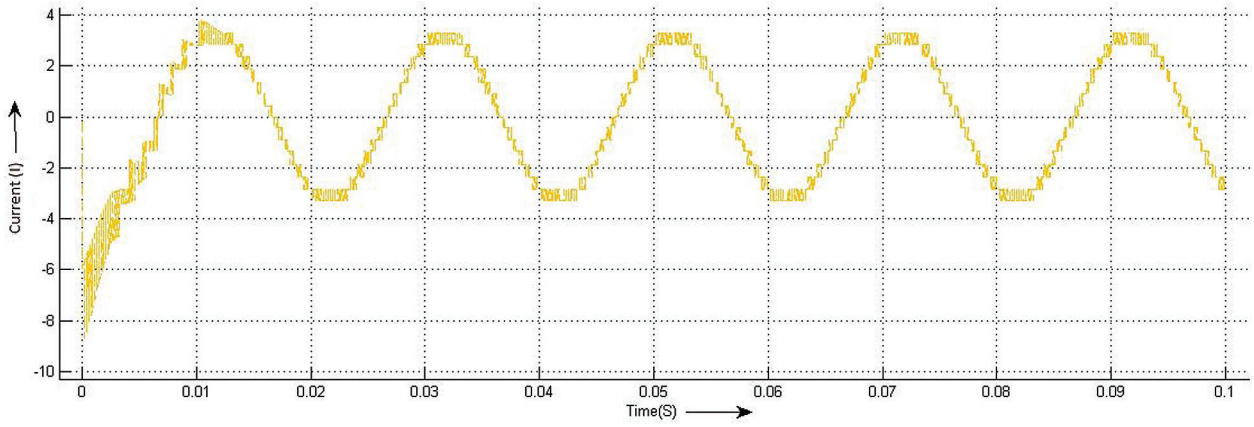

Figure 9: Output (Level generation unit and H bridge) current

Fig. 8 illustrates the inverter output voltage of level generation unit and the common H Bridge. As a steady-state response, the current waveform for a resistive load is also shown in Fig. 9. In this case, the *f*s is kHz with the output frequency of 50 Hz.

Simulation results show that the line-to-neutral voltage THD is 6.73% for the proposed 15 level CDDCLC. This confirms the improved power quality of increased output voltage.

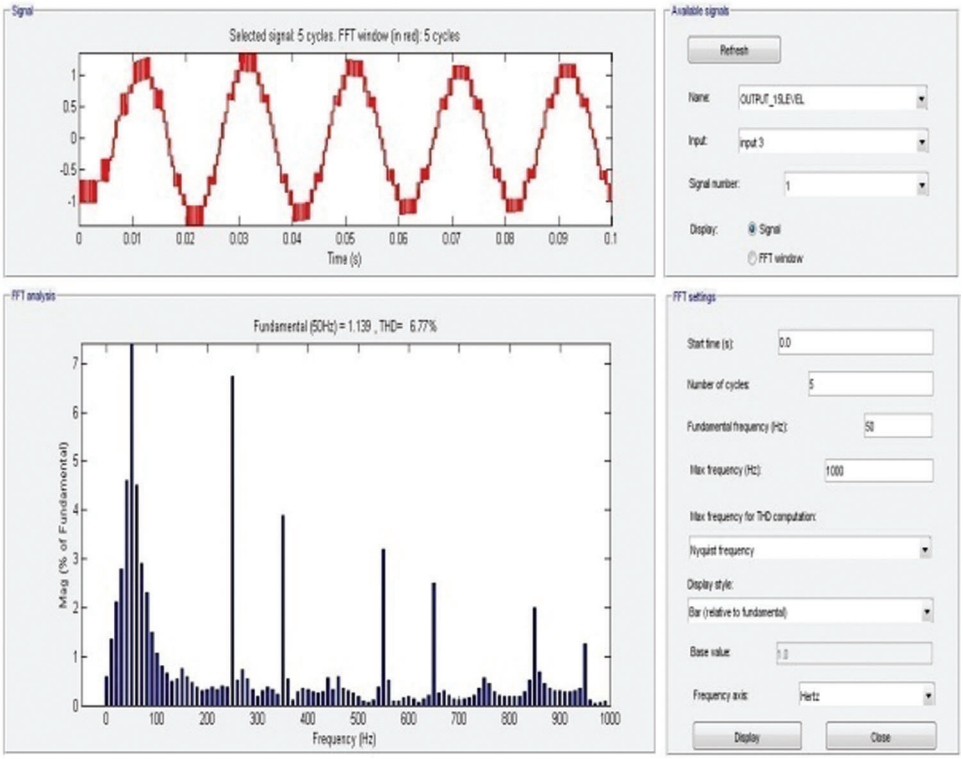

Figure 10: FFT analysis of proposed 15 levels CDDCLC

Table 2: Simulation parameters of 15 level CDDCLC

Parameter	Value
PV voltage	12 V
Boost chopper voltage	28 V
DC-Link voltage	60 V
Output RMS voltage	42 V
Load	30 Ohms
Output frequency	50 Hz

6 Comparison of Hardware System Design

A CDDCLC from the DC input to AC output mainly consists of three parts: a chopper, a level generation unit, and common H Bridge. The power loss of the CDDCLC originates from the three parts. The IGBTs are selected for the chopper and multilevel inverter. Most of the power loss in the CDDCLC is due to the switching loss and the conduction loss of the IGBTs and diodes. The 1Ø CDDCLC configuration is intended and applied for 150 V (Vmax) output voltages. It is observed that the Controller and driver unit with CDDCLC constitute the implementation setup. Further, the DC input for the lift chopper units is derived from the supply of rectifier and battery banks. Here, the boost chopper is made up of HGTG20N100D2 insulated gate bipolar transistor (IGBT) switches and passive components (L1 = L2 = 2 mH and C1 = C2 = 100 μF). Tab. 3 represents the technical specifications of HGTG20N100D2 power IGBT and driver ICTLP250. Fig. 11 shows the experimental setup.

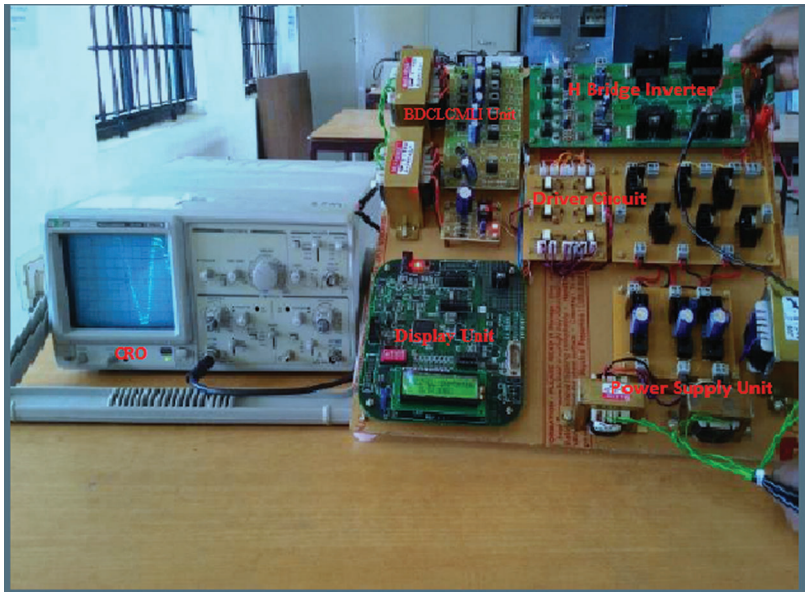

Figure 11: Experimental setup

The control signs to the IGBT driver circuit are given by the microcontroller (ATmega328). The driver circuit is designed using the driver IC from Toshiba-TLP250. HGTG20N100D2 power IGBT switches used in fabricating the DCLM and H-bridge inverter systems. Isolation and amplification processes are provided by the driver circuit using TLP250. Tab. 4 shows the technical specifications of driver IC TLP250.

Table 3: IGBT specifications

Symbol	Test conditions	Maximum ratings
V_{CES}	$T_J = 25\,°C$ to $150\,°C$	1000 V
V_{CGR}	$T_J = 25\,°C$ to $150\,°C$, $R_{GE} = 1\,M\Omega$	1000 V
V_{GES}	Continuous	±20 V
V_{GEM}	Transient	±30 V
I_{C25}	$T_C = 25\,°C$	40 A
I_{C90}	$T_C = 90\,°C$	20 A
I_{CM}	$T_C = 25\,°C$, 1 ms	100 A

Table 4: Driver IC specifications

S.no	Parameters	Specifications
1	Input threshold current	5 mA (max)
2	Supply Current	11 mA (max)
3	Supply voltage	10–35 V
4	Output Current	±1.5 A (max)
5	Switching time t_{pLH}/t_{pHL}	0.5 μs (max)
6	Isolation voltage	2500 Vrms (min)

The hardware results show that the line-to-neutral voltage is 139.9 V as shown in Fig. 12 and the THD is 9.7% as shown in Fig. 13 for the proposed 15 level CDDCLC. It shows the improved power quality performance of output voltage.

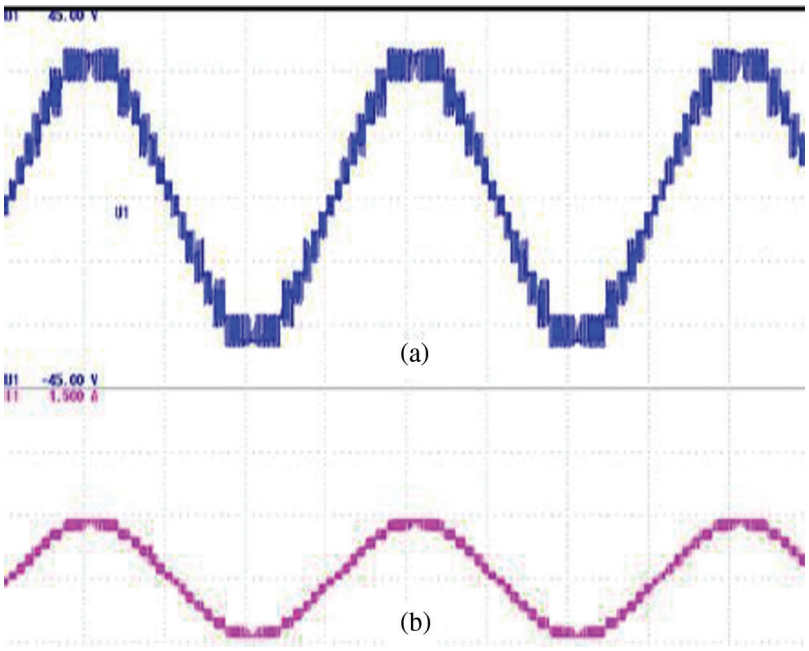

Figure 12: Fifteen level Inverter (a) Output voltage & (b) Output current for R Load

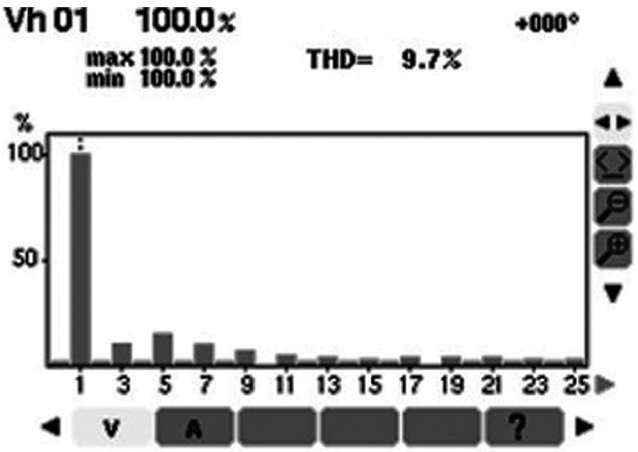

Figure 13: Voltage THD

Fig. 12 illustrates the output voltage and current waveform of inverter circuit with R Load.

Fig. 13 illustrates the Voltage THD harmonic profile for Proposed topology.

Fig. 14 illustrates the output voltage and current waveform of inverter circuit. The inverter independently generates the desired fifteen level output voltage and current. Tab. 5 shows the correlation of proposed geography with that of other papers mentioned in literature. When compared with other four research papers the work proposed in CDDCLC gives better results. It requires just 10 switches for

accomplishing 15 levels. Fig. 16 also shows the qualitative analysis of proposed CDDCLC work. Tab. 6 shows the correlation of proposed geography with that of other papers mentioned in literature. It requires just 3 DC sources for accomplishing 15 levels.

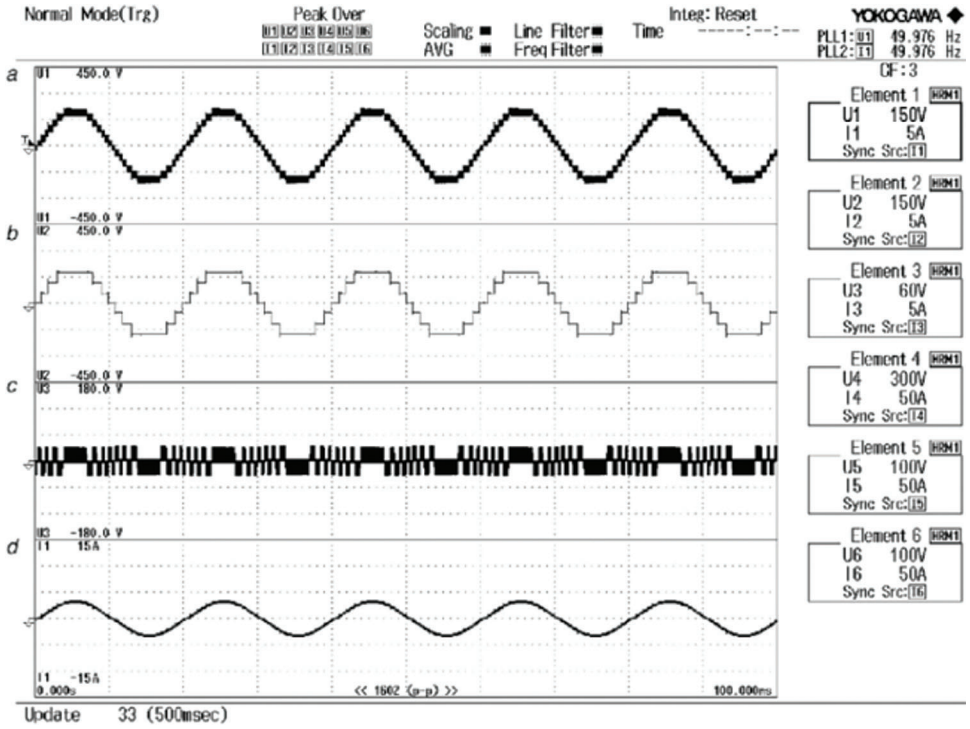

Figure 14: Output voltage and current waveform

Table 5: Switch tally examination

Levels	CMLI	BCMLI	BDCLCMLI	Proposed BDCLCMLI
5	8	10	7	6
7	12	15	10	8
15	28	35	13	10
31	60	75	16	12

Tab. 7 shows simulated harmonic analysis of proposed BDCLCMLI. From the examination voltage harmonics from 8.45%(BDCLCMLI) to 6.73%(Proposed BDCLCMLI). Fig. 15 illustrates the qualitative analysis of proposed BDCLCMLI with other relevant works. The chart demonstrates the improvement of boundaries to be specific number switches, number of sources and voltage stress.

Fig. 16 illustrates the voltage harmonic analysis of proposed BDCLCMLI for R load. The diagram shows the voltage THD for different recurrence adjustment record esteems are investigated.

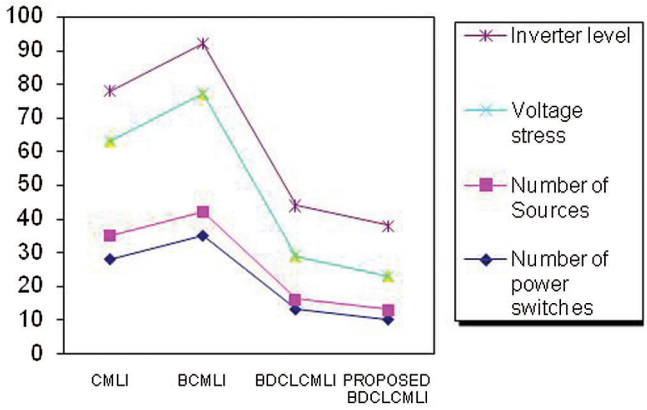

Figure 15: Line chart base qualitative analysis of proposed BDCLCMLI with other works

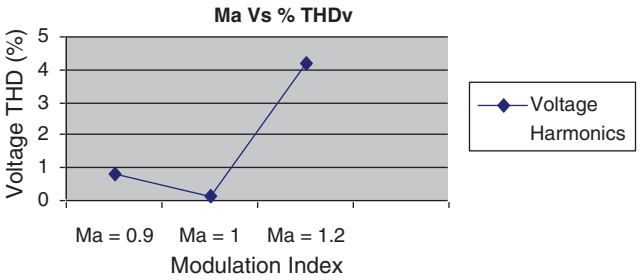

Figure 16: Voltage harmonic analysis of proposed BDCLCMLI (for R Load Vs = 230 V)

Table 6: DC sources examination

Levels	CMLI	BCMLI	BDCLCMLI	Proposed BDCLCMLI
5	2	2	1	1
7	3	3	2	2
15	7	7	3	3
31	15	15	4	4

Table 7: Harmonic analysis of proposed BDCLCMLI (For R LOAD Vs = 230 V)

Order of harmonics	Ma = 0.9		Ma = 1.0		Ma = 1.2	
	Voltage harmonics %	Current harmonics %	Voltage harmonics %	Current harmonics %	Voltage harmonics %	Current harmonics %
3	0.8	0.8	0.12	0.12	4.2	4.2
5	0.05	0.05	0.45	0.45	3.2	2.2
7	0.1	0.03	0.36	0.07	0.07	0.04
9	0.6	0.06	0.05	0.04	0.03	0.06
11	0.07	0.3	0.17	0.03	0.34	0.03
13	0.03	0.02	0.26	0.07	0.03	0.02
15	0.04	0.07	0.34	0.02	0.23	0.06

7 Conclusion

In this paper single-stage fifteen levels DC-interface converter (CDDCLC) is proposed for sun oriented photovoltaic (PV) applications. The proposed topology is incorporated with support DC chopper and H-connect inverter to optimize the power converter to achieve the minimum harmonic profile. In examination with the traditional inverter frameworks, the proposed framework is utilized with decreased voltage stress, reduced switch check and DC source count. The proposed research work with CDDCLC configuration requires three DC sources for synthesizing fifteen-level AC output. This exploration structure is emphatically suggested for power converters utilized in UPS and drive applications since it is very economical. A reproduction and model of fifteen-level CDDCLC geography shows its total execution. This investigation structure switching technique is phase opposition and disposition pulse width modulation technique (POPD) which results in improved quality of obtained output AC power with 6.73% THD.

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