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Design of Precise Multiplier Using Inexact Compressor for Digital Signal Processing

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Abstract: In the recent years, error recovery circuits in optimized data path units are adopted with approximate computing methodology. In this paper the novel multipliers have effective utilization in the newly proposed two different 4:2 approximate compressors that generate Error free Sum (ES) and Error free Carry (EC). Proposed ES and Proposed EC in 4:2 compressors are used for performing Partial Product (PP) compression. The structural arrangement utilizes Dadda structure based PP. Due to the regularity of PP arrangement Dadda multiplier is chosen for compressor implementation that favors easy standard cell ASIC design. In this, the proposed compression idealogy are more effective in the smallest *n* columns, and the accurate compressor in the remaining most significant columns. This limits the error in the multiplier output to be not more than 2^n for an n X n multiplication. The choice among the proposed compressors is decided based on the significance of the sum and carry signals on the multiplier result. As an enhancement to the proposed multiplier, we introduce two Area Efficient (AE) variants viz., Proposed-AE (P-AE), and P-AE with Error Recovery (P-AEER). The proposed basic P-AE, and P-AEER designs exhibit 46.7%, 52.9%, and 52.7% PDP reduction respectively when compared to an approximate multiplier of minimal error type and are designed with 90nm ASIC technology. The proposed design and their performance validation are done by using Cadence Encounter. The performance evaluations are carried out using cadence encounter with 90nm ASIC technology. The proposed-basic P-AEA and P-AEER designs demonstrate 46.7%, 52.9% and 52.7% PDP reduction compared to the minimal error approximate multiplier. The proposed multiplier is implemented in digital image processing which revealed 0.9810 Structural SIMilarity Index (SSIM), to the least, and less than 3% deviation in ECG signal processing application.

Keywords: Approximate computing; precise multiplier; PP compression; area-efficient; error-recovery approach

1 Introduction

The process of multiplication and addition are the essential functions carried out by the Arithmetic Unit (AU). Basic elements of the processing applications like signal, Image and multimedia process are formed by using Arithmetic Units (AU). The operating frequency of the processing relies on AUs critical delay and depends on the setback of multiplier. The operating frequency for processing element is determined AUs critical delay which relies on the delay of the multiplier. Array multiplication is the standard algorithm used to multiply 2 input operands that use parallel approach for PP generation. The PP bits are shifted based on weight and compressed using Carry Propagate Adder (CPA).

Scaling at deep submicron technology increases the density of integration in VLSI chips. Hence the power density increases proportionately, and the heat dissipation issues arise. Low supply voltage operation to solve the power density issues, on the other hand, increases delay. A number of approaches to the design of multipliers for optimum performance are proposed in the literature. Low error and area-efficient truncated multipliers are proposed for fixed-width applications [1–6]. In [7], a multiplexer based array multiplier is proposed with new adaptive PCT (Pseudo-carry Compensation Truncation) scheme. A low complexity multiplier using a pipelined parallel counter is proposed in [8].

Approximate computing is a recent methodology for the logic design of high speed, reduced power and area-efficient architectures for approximate applications. Approaches to the design of area and power-efficient approximate adders are proposed in [9–12]. Memristor based approximate full adder [13] and configurable accuracy error tolerant adder [14] are proposed for PP compression in multipliers. A reduced-cost imprecise multiplier employing probability–driven imprecise compressor and inexact half-adder is proposed in [15]. Approaches to the design of inexact compressors are proposed in [16–22], and approximate multipliers employing inexact compressors are proposed in [23–25] targeting error-tolerant applications. Adaptable multipliers with flexibility in switching between exact and approximate modes are proposed using Dual mode compressor [26], variable approximation mode compressor with error recovery, and ultra-low power compressor [27]. A high-speed multiplier employing reduced critical path node capacitance approximate compressor is proposed in [28–31]. In [32], a probabilistic based approach for PP accumulation based on significant bit position is proposed to minimize logic complexity and power dissipation. Low-error high-speed Wallace multiplier with inexact 4:2 compressor and error-correction circuit has newly developed in [33]. For a need based error-tolerant application, multipliers are being designed with energy error trade off [34,35], and multi-level approximation [36].

In this approach, two novel approximate 4:2 compressors were proposed that can optimize area, power, delay, and generate either sum or carry with no error. The proposed compressors are targeted for PP compression in multipliers with structure-based PP arrangement that employ Dadda multipliers. In the targeted multipliers, for $n \times n$ design, the proposed inexact compression highly appreciable in the least n significant(LS) columns and exact 4:2 compressor in the remaining most significant(MS) Partial Product arrangements. The choice among the proposed compressors in PP columns of the approximate part depends on the significance of compressor output signals on the multiplier result. Least significant n columns of multiplier are employed with approximate multipliers that bound the maximum error in the output not more than 2^n. If the error in the output is being reduced less than 2^n then it can be considered as a tolerable level. With the reduced errors, these multipliers are specially suited for error-recovery applications can be utilized in image and signal processing. Area efficiency and speed improvement in the proposed precise multiplier are achieved by non- generation of carry signals for the final stage in the approximate part. Furthermore, to reduce error due to non-generation of carry signals in the area efficient version of the proposed multiplier, we generate error recovery compensation bias using pre-final stage carry signals of n/4 most significant columns in the approximate part and add it to the least significant carry signal of the exact part in the final stage. Novelty and functional verification of the proposed multipliers are done by implementations with Image smoothing and ECG signal processing applications.

In this paper, Section 2 presents a typical 4:2 exact compressor with structural modifications. Section 3 describes about the design and its functionality in the sense of speed in all aspects of multiplication. The performance of the above said novelties are evaluated in Section 4. Section 5 details the newly up to date characteristics multiplier in various digital technology deployments. As a final note, a comprehensive assumption of the behind the proposed work is presented in Section 6.

2 Exact and Other Inexact Compressors

4:2 compressor is one of the perfect choice to perform PP compression in multipliers for the arithmetic units with fixed width data path of 2 (i.e., 2N where N = 3, 4, 5, 6) as its multiplying number likewise as exactly similar to Arithmetic unit of the processors is the major advantage in all kinds of digital technology deployment as Partial Product compression concerned with firm-width data path. The implementation of the compressor is through Dadda type multiplier because of regularity in the PP arrangement that favors easy standard cell ASIC design. In the sub Section 2.1, proposed 4:2compressor and design of approximate compressors are explained.

2.1 Exact Compressor

By using exact compressor, the n 1-bit inputs are added, where n is equal to the functionality $n < 2^i$, which results to '*i*' that is first integer and '*n*' is the last integer. A conventional 4:2 compressor having A_1, A_2, A_3, A_4 as four inputs along with C_i as the previous balance carry which generates Sum, Carry, C_o in its output. The architecture and its Boolean expressions can be formulated in Fig. 1 and Eqs. (1)–(3) respectively.

$$S = A1^{\wedge}A2^{\wedge}A3^{\wedge}A4^{\wedge}Ci \tag{1}$$

$$C = [(A1^{\wedge}A2)\ \&\ A3]||[(A1^{\wedge}A2)'\ \&\ A1] \tag{2}$$

$$C_O = [(A1^{\wedge}A2^{\wedge}A3^{\wedge}A4)\ \&\ Ci]||[(A1^{\wedge}A2^{\wedge}A3^{\wedge}A4)'\ \&\ A4] \tag{3}$$

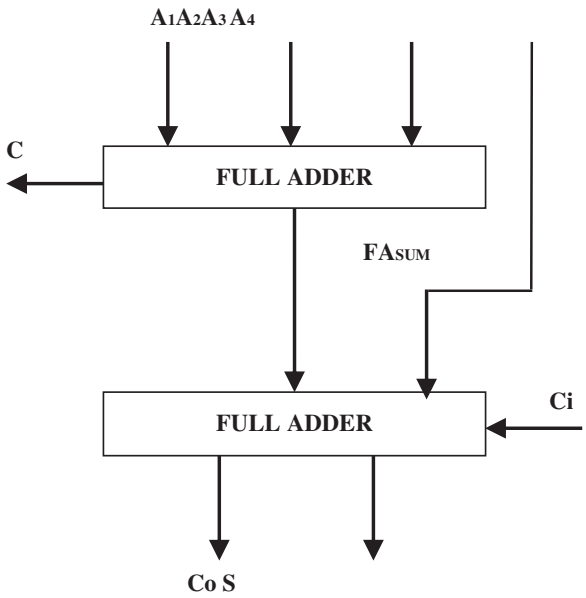


Figure 1: Block-levelfigure. Exact 4:2 compressor

The standard Boolean expression the compressor is modified for Partial Product compression of multipliers as logic low in C_i and output C_o is ignored. The proposed 4:2 new compressor has same inputs as stated above and Sum-S and Carry-C as the outputs. The ignorance of C_o in the new compressor causes error when $A_1A_2A_3A_4$ = "1111" has probability.06 and Maximal Error Deviance that is (Max-ED) = −2.

Contrarily, the algorithm of approximation which generates *Sum* for logic high as $A_1A_2A_3A_4$ = "1111" minimize the Max-ED to −1. The block level figure of the modified exact compressor is shown in Fig. 2, and related Boolean expression shown in Eqs. (4), (5).

$$S = A1^{\wedge}A2^{\wedge}A3^{\wedge}A4 \tag{4}$$

$$C = ((A1^{\wedge}A2^{\wedge}A3^{\wedge}A4)' \ \& \ A4) \tag{5}$$

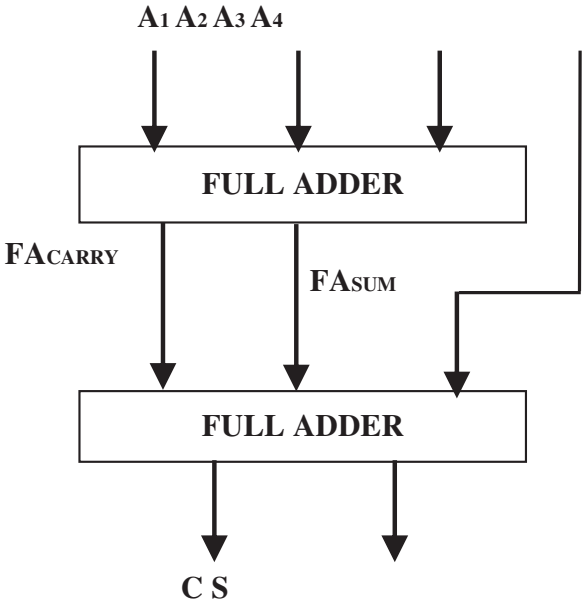


Figure 2: Block level figure. Modified exact 4:2 compressor

The delay of computation for AND, OR, XOR, NOT, XNOR, and NAND gates are denoted as t_{AND}; t_{OR}; t_{XOR}; t_{NOT}; t_{XNOR}; *and,* t_{NAND}, respectively. Based on this, logic depth is calculated by counting the number of gates in critical path of the design. The logic-depth of modified 4:2 exact compressor is given as $t_{logic\text{-}depth} = 3 * t_{AND} + 3 * t_{OR}$.

However, in the multiplier implementation of projected circuit explained in Section 3, we considered C_o as ignored in the projected circuit has been compensated to eliminate error by adding bit $E = A_1\&A_2\&A_3 \ \& \ A_4$.

3 Proposed Multiplier Using Inexact Compressors

3.1 Design of Inexact Compressors

This section briefs the design of efficient approximate 4:2 compressors that can generate either sum or carry with no error. In proposed design 1, the logic generates no error in sum and three errors in carry, and it will be referred hereafter as "Proposed compressor with Exact Sum" (Proposed-ES). In proposed design 2, the logic generates no error in carry and three errors in sum, and it will be referred hereafter as a Proposed

compressor with Exact Carry(Proposed-EC).As the target for our approximate compressors is to design high-speed multipliers with reduced error, the proposed compressors are used in PP compression logic based on the significance of compressor sum and carry signals on the multiplier output.

3.1.1 Proposed-ES Design

In the proposed-ES design shown in Fig. 3, single bit FA cell takes in three inputs K_1, K_2, K_3, and produce the sum signal (FA_{sum}). Exact sum and error-prone carry outputs of the denoted as S and C' to make separate identity from exact output. The logic that implements S and C' outputs of the Proposed-ES variant by Eqs. (6)–(8).

$$FA_{sum} = (A1 \hat{} A2) \hat{} A3 \tag{6}$$

$$S = FA_{sum} \hat{} A4 \tag{7}$$

$$C' = (\sim FA_{sum}) | A4 \tag{8}$$

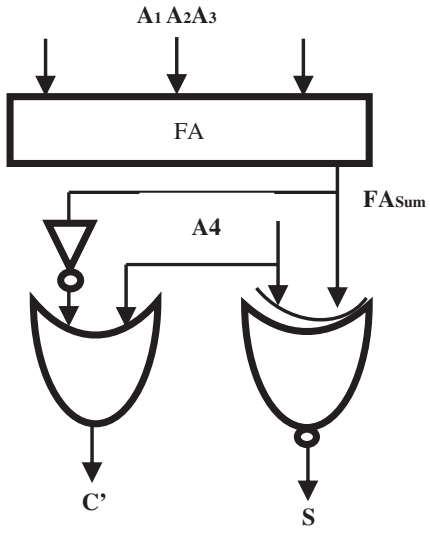


Figure 3: Logic diagram of proposed-ES compressor

In reference to the Boolean Eqs. (6), (7), that the Proposed-ES compressor introduces no error in S and three errors in C' for "$A_4A_3A_2A_1$ = "0000", "0111" & "1000" with error proportion 0.1875. Also, it is noted that the MES of the Proposed-ES design for inputs $A_4A_3A_2A_1$ = "0000", "0111", "1000" & "1111" is ±2. However, this MES will not affect the performance of multipliers incorporating the Proposed-ES compressor, as it is used only in PP columns where sum signal has a stronger influence on the multiplier output. The logic-depth of Proposed-ES design is stated by $t_{Prop\text{-}ES} = 2 * tx_{OR} + 1 * t_{OR}$.

3.1.2 Proposed-EC Design

In the Proposed-EC design shown in Fig. 4, there are three inputs A_1, A_2, A_3 for single bit approximate FA (AFA) that generates the approximate carry denoted as (AFA_{carry}) and approximate sum denoted as (AFA_{Sum}) signals as outputs. The sum output is notified as S' to make difference from the exact sum S, and the carry output is C. The boolean expressions that implement S' and C outputs of the Proposed-EC design are stated by Eqs. (11), (12).

$$AFA_{carry} = (A1\&A2) | (A2\&A3) | (A1\&A3) \tag{9}$$

$$AFA_{sum} = (A1|A2)|A3 \tag{10}$$

$$S' = \sim (AFA_{carry}{}^{\wedge}A4) \tag{11}$$

$$C = (AFA_{carry} \ \& \ (\sim A4))|(AFA_{sum}\&A4) \tag{12}$$

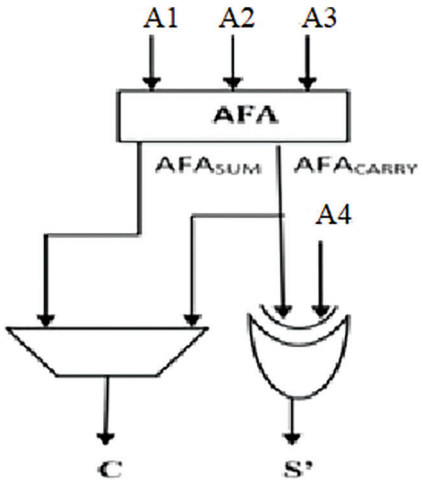


Figure 4: Logic diagram of proposed-ECcompressor

It is well known from the Boolean Eqs. (11) and (12), Proposed-EC design produces three sum errors found for inputs $A_4A_3A_2A_1$ = 10000, 0111 & 0000 and proportion of error to be 0.1875, and no error in carry. For the input "1111", the value of error considered as negligible since it minimizes MES to −1. The compressed partial product probability on MES logic signal is 0.06, and it does not affects the performance of the new variant multipliers since the output approximation to be not more than 2^n compared with exact signals. The target use of the Proposed-EC design is in PP columns where the carry signals are more significant than the multiplier output.

The Proposed-EC compressors logic depth is $t_{Prop\text{-}EC} = 2 * t_{XOR} + 1 * t_{OR}$

3.2 Design of Precise Approximate Multiplier

This section briefs the design of $n \times n$ precise approximate multiplier that uses proposed approximate compressors for n least significant columns and exact 4:2 compressor for the remaining most significant PP columns. The PP compressions are performed in several stages with Dadda structure-based PP arrangement by using multipliers and carry save addition. In the final stage, the RCA is employed to perform final addition. The maximum imprecise compressor error in the $2n$ bit multiplier confined to one unit in Bit Significant Position (BSP) − n (i.e., 2^n). Fig. 5 illustrates the new methodology in n = 8 bits as the input operators of the multiplier as a [7:0] and b [7:0]. Generated PP bits are arranged in Dadda structure to reduce complexity, and number of Partial Product compression to be done in four levels. Since the carry logic has a higher significance over sum, the Proposed-EC compressor is used in the approximate part, and the modified exact 4:2 compressor is used in the accurate part of the multiplier. Note that the modified exact 4:2 compressor introduces error. For the input = "1111", the new variant 4:2 compressor precedes free from error by adding the compensation bit $-E_{ji}$ is added for reimbursement in the MS column. The Boolean expression of E_{ji} is

$$E_{ji} = (A1\&A2)\ \&\ (A3\&A4) \tag{13}$$

where '*i*' represents stage number in PP compression, and 'j' represents column weight. Fig. 6 shows architecture at gate level for parallel computation of $E_{1\text{-}12}$ and $E_{1\text{-}13}$. This assures that the error compensation in stage-1 due to the modified exact compressor doesn't acquaint with additional delay on the PP compression. In the final stage, sum and carry signals are added using 16 bit RCA. To trade-off area and delay for accuracy in the proposed basic version, we perform final stage addition using two different methodologies. A detailed description of the structural modifications in the proposed multiplier is discussed in subsections 3.2.1 and 3.2.2. In all the proposed multiplier designs for adding 2 and 3 bits, approximation Half Adder (AHA), and approximation Full Adder (AFA) cells are used in LS part and exact adders in the MS part. The expressions for carry and sum outputs of these two adders are given by Eqs. (14) and (15), respectively.

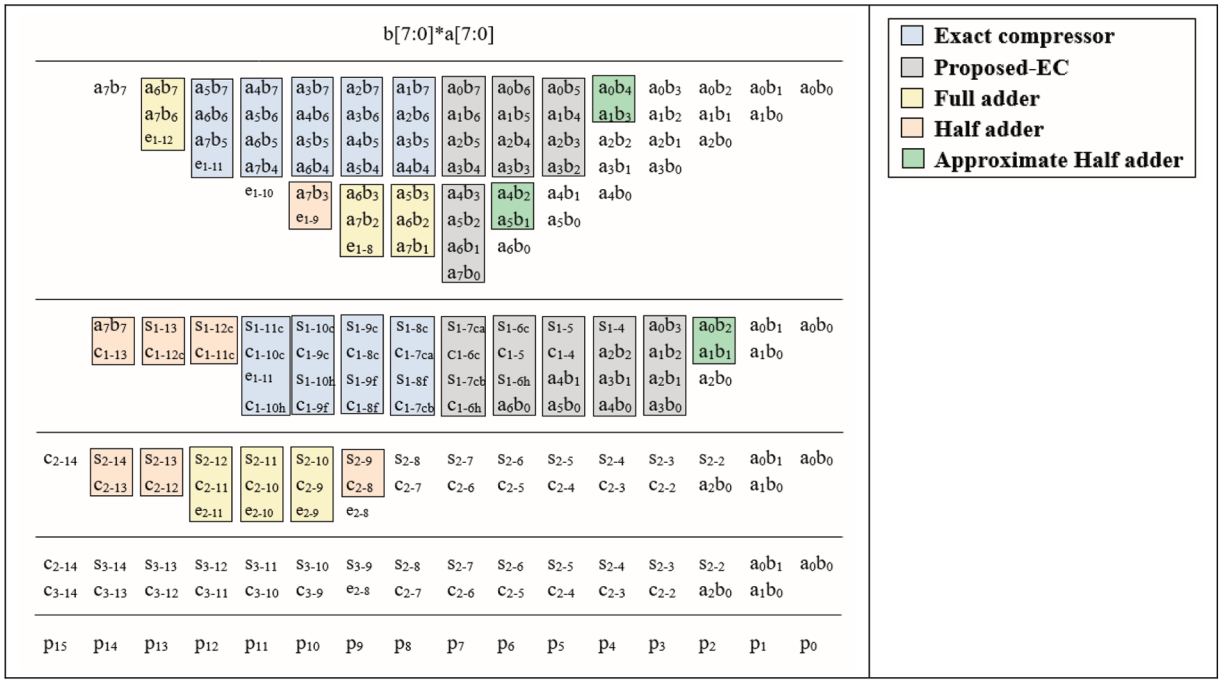


Figure 5: PP compression in proposed multiplier

$$AHA_{Carry} = a\ \&\ b$$

$$AHA_{sum} = \sim AHA_{carry} \tag{14}$$

$$AFA_{carry} = a\ \&\ b\ \&\ c$$

$$AFA_{sum} = \sim AFA_{carry} \tag{15}$$

3.2.1 Proposed–AE Design

In the Area Efficient (AE) design designated as Proposed-AE(P-AE), carry bits are not generated in LS imprecise part of the final stage, and MS bits adding of the exact part is performed using *n* bit RCA. Fig. 7 shows the PP compression using 4:2 compressors, and final stage addition in the P-AE multiplier for $n = 8$.

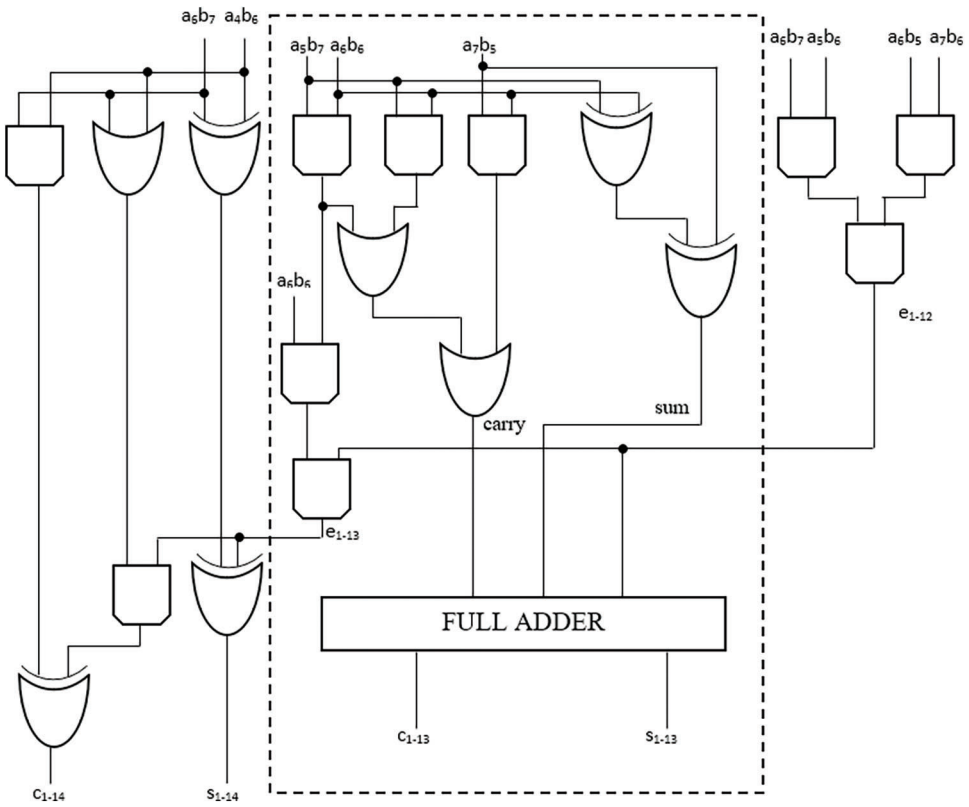


Figure 6: Gate level architecture for parallel computation of $E_{1\text{-}12}$ and $E_{1\text{-}13}$

Note that we use the Proposed-EC compressor in the approximate part in stage-1 since carry signal has a greater influence in stage-2 and on the multiplier output. In stage-2, we use the Proposed-ES compressor for columns with binary weight 3–6, as the influence of the sum signal is higher in these columns on the multiplier output. However, for the column with binary weight 7, we use the Proposed-EC compressor as the carry signal in this column has higher significance on the final result. Note from Fig. 7 that the P-AE multiplier uses n bit RCA in the final stage, which reduces delay and area considerably by a little contraction in its precision. Conversely, the maximum error in the P-AE multiplier due to approximation restrains to 1 unit at BSP n (i.e., 2^n).

3.2.2 Proposed–AEER Design

In the Proposed Area Efficient with Error Recovery multiplier (P-AEER), carry bits are generated in the most significant two PP columns of the approximate part in the pre-final stage. An error recovery (E_R) signal is generated using AND logic on these carry bits and is added with the least significant carry signal in the accurate part. The logic of E_R is given by Eq. (16).

$$E_R = C_{2-7} + C_{2-6} \ \& \ C_{2-5} \tag{16}$$

Symbols + and & represents arithmetic OR and logical AND operations, respectively. Fig. 8 shows the PP compression in P-AEER design using exact and proposed 4:2 compressors for $n = 8$. Note from Fig. 8, for the final stage addition, we use only n bit RCA in the most significant part, and it reduces the delay in carry propagation significantly. Hence, the P-AEER multiplier achieves better area and delay reductions compared to the basic version and fair better improvement in average error compared to P-AE design.

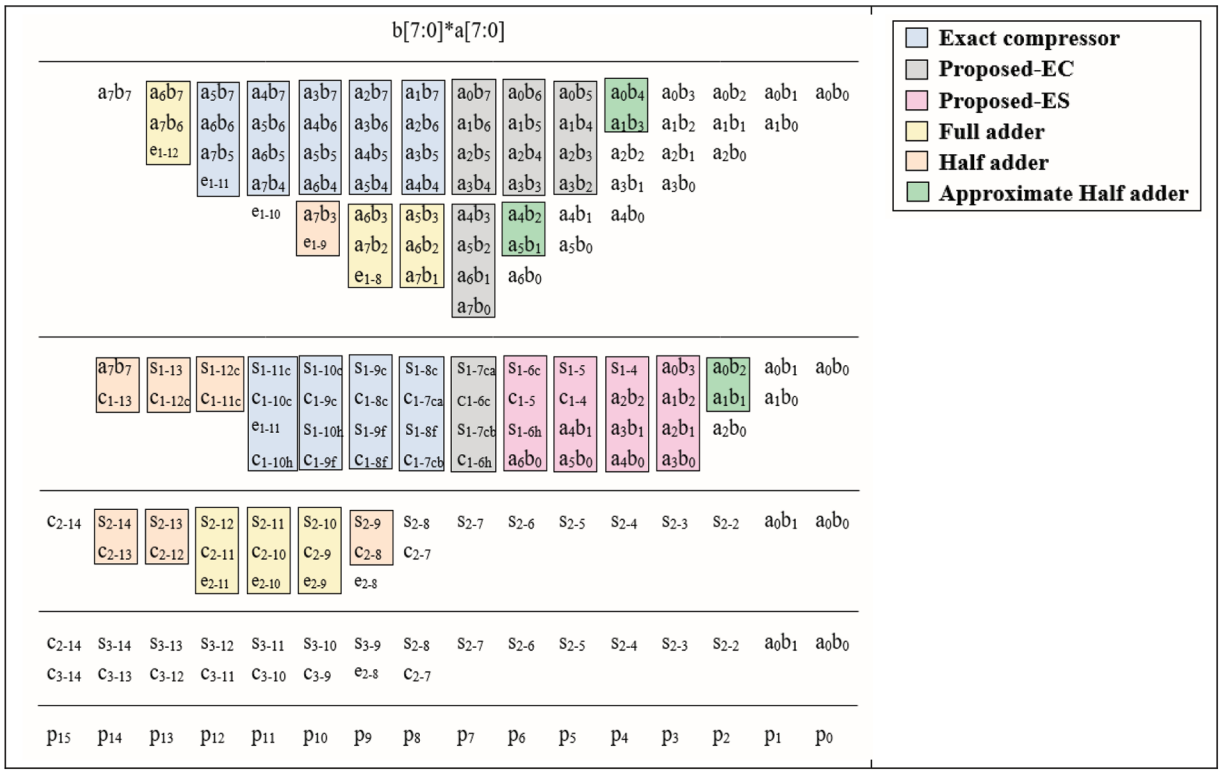


Figure 7: PP compression in P-AE multiplier

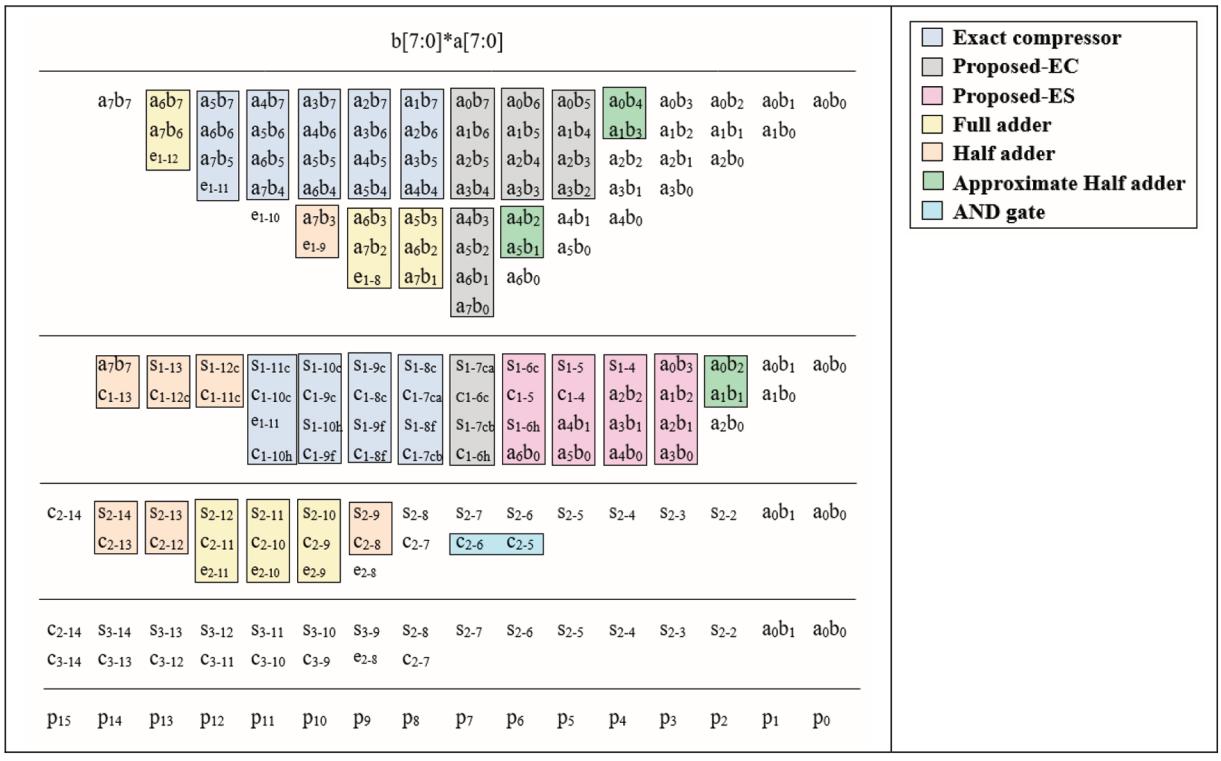


Figure 8: PP compression in P-AEER multiplier

Tab. 1 shows E_R for various combinations of signals used in the error recovery in P-AEER design. However, the maximum error in P-AEER multiplier restrains to 1 unit at BSP n (i.e., 2^n).

Table 1: E_R in P-AEER design for various combination of carry signals

Case	1	2	3	4
$S_{2\text{-}7}\ S_{2\text{-}6}$	00	01	10	11
$C_{2\text{-}6}\ C_{2\text{-}5}$	11	11	11	11
Error	2^6	2^6	2^6	2^6
E_R	2^7	2^7	2^6	2^6

4 Results and Discussion

The novel multipliers, inexact compressors and its design are explained in the review of literature section and are designed using structural Verilog HDL codes. The multipliers are synthesized using Cadence Encounter in 90nm technology. To optimize supply voltage for simulations, we made a performance estimate of the proposed compressor design in terms of power and delay, and found that at supply voltage-1 V, the PDP of proposed compressors is low, and hence performance comparison of multipliers with new variant compressors and the novel multiplier variants is made using simulations with supply voltage-1 V.

4.1 Approximate Compressors Performance Comparison

Performance metrics in terms of power, area, delay, and PDP of proposed compressors and state-of-the-art approximate designs used for comparison are shown in Tab. 2. The metrics are estimated at operating frequency-200 MHz, and supply voltage–1V. We have used exact compressor as the standard for error comparison of all approximate approaches. Note that from Tab. 2, Proposed-ES and Proposed-EC designs demonstrates 26.8% & 42.4%, 60.4% & 68.9%, 9.6% & 28.9%, 14.4% & 32.7% power reductions, and 25.7% & 22.9%, 51.9% & 50%, 16.1% & 12.9%, 18.8% & 15.6% area reductions, respectively compared to Exact, and compressors in XOR-XNOR module, Modified architecture of Dadda Multiplier, Imprecise 4-2 compressor. Compressor designs in Two approximate 4-2 compressors (TA4-2C), 4-2 compressor-based approximate multiplier (4-2CAM), DQ4:2C3 fair better power dissipation compared to the proposed designs, while the total error generated by these designs is significantly high compared to the proposed designs. In terms of PDP, Proposed-ES and Proposed-EC designs demonstrates 51.5% & 59.3%, 69.4% & 74.4%, 14.9% & 28.7%, and 19.7% & 32.7% reductions compared to Exact, XOR-XNOR module, modified architecture of Dadda Multiplier (MADM), and imprecise 4-2 compressors (I4-2C), respectively. Approximate multiplier with adder and DQ4:2C3 compressors generate carry output directly from Cin and X4 respectively. Hence in HDL modeling, a buffer is used for the generation of carry signals in these designs. Hence PDP of compressors in Approximate multiplier with adder and DQ4:2C3 are significantly low compared to Exact, designs in XOR-XNOR module, modified architecture of Dadda Multiplier, imprecise 4-2 compressor and proposed compressors. Approximate compressor in 4-2 compressor-based approximate multiplier demonstrates the lowest PDP compared to all other designs considered. It is due to the parallel design of logic that reduces delay significantly but at the expense of 5 errors.

Table 2: Performance comparison for proposed multiplier with prior designs

Compressors	Power (nw)	Area ($\times 10^{-6}$ m^2)	Delay (ps)	PDP ($\times 10^{-16}$ Joules)	Error	
					Carry	Sum
Exact design	1597	35	708	11.31	–	–
XOR-XNOR	2957	54	607	17.95	3	0
TA4-2C	519	18	222	1.152	2	3
DQ4:2C3	836	20	220	1.84	5	5
4-2CAM	549	17	192	1.05	2	3
MADM	1293	31	499	6.45	1	1
I4-2C	1366	32	501	6.84	4	4
Proposed-ES	1169	26	470	5.49	3	0
Proposed-EC	919	27	501	4.60	0	3

4.2 Results of Precise Approximate Multiplier

4.2.1 Error Metrics

Error metrics are the important parameters to evaluate the efficacy of an approximate design in error-tolerant applications. In this section, the performance of the proposed approximate multipliers and state-of-the-art approximate designs is evaluated in terms of various error metrics Modified architecture of Dadda Multiplier, 4-2 compressor-based approximate multiplier, DQ4:2C3 using standard output as the recent works. The accuracy metrics considered are Mean Error Distance (MED), Mean Relative Error Distance (MRED), Normalized Error Distance(NED), and Percentage Accuracy. Tab. 3 shows the MED, MRED, and NED values of proposed and prior multiplier designs. It is noted from Tab. 3, MED values of our basic, AE, and AEER designs are considerably low compared to approximate multipliers in 4-2 compressor-based approximate multiplier, DQ4:2C1, DQ4:2C2, DQ4:2C3, and Modified architecture of Dadda Multiplier, thanks to the proposed compressor designs that reduce the signal error probability that influences multiplier output. Moreover, the modified exact 4:2 compressors used in most significant n PP columns and compensation bit added to bias the error for the input "1111", maintains the error precisely within 2^n. Consistently, MRED and NED values of proposed multipliers are relatively low compared to approximate multipliers in 4-2 compressor-based approximate multiplier, DQ4:2C1, DQ4:2C2, DQ4:2C3, and Modified architecture of Dadda Multiplier.

Table 3: Comparison of error metrics with the proposed multipliers and prior designs for $n = 8$

4-2CAM	DQ4:2C1	DQ4:2C2	DQ4:2C3	DQ4:2C4	MADM	I4-2C	Proposed	P-AE	P-AEER	4-2CAM
348	899	427.5	951.8	401.5	320.3	118.6	121.4	129.7	128.1	348
0.13	0.22	0.13	0.22	0.10	0.07	0.019	0.02	0.03	0.03	0.13
0.14	0.20	0.10	0.22	0.13	0.09	0.02	0.03	0.02	0.04	0.14

4.2.2 Power, Delay, Area Comparison

Performance of the proposed and state-of-the-art multipliers in terms of total power dissipation (power), area, delay and PDP are shown in Tab. 4. From Tab. 4, the static power dissipations of proposed designs are significantly improved compared to multipliers in DQ4:2C4, Imprecise 4-2 compressor and exact multipliers.

Total power dissipation of Proposed-basic, P-AE and P-AEER multipliers are 8%, 13.7%, 13.4%; 2.9%, 8.9%, 8.7%; and 27.6%, 32%, 31.8% reduced compared to multipliers in Modified architecture of Dadda Multiplier, DQ4:2C4,Imprecise 4-2 compressor, while multipliers in 4-2 compressor-based approximate multiplier, DQ4:2C1, DQ4:2C2, DQ4:2C3 exhibit betterpower performance. Conversely, the error percentage of multipliers in 4-2 compressor-based approximate multiplier, DQ4:2C1, DQ4:2C2, DQ4:2C3 are at the least 10.1%, 19.42%, 10.7%, and 19.58% high compared to the proposed designs. Proposed-basic, P-AE and P-AEER multipliers demonstrates 6.8%, 12.1%, 12.1%; 6.3%, 11.6%, 11.6%; 6.3%, 11.6%, 11.6%; 8.5%, 13.7%, 13.7%; 11.6%, 16.6%, 16.6%; 9.5%, 14.7%, 14.7%; and 26.5%, 30.6%, 30.6% low delay compared to multipliers in 4-2 compressor-based approximate multiplier, DQ4:2C1, DQ4:2C2, DQ4:2C3, DQ4:2C4, Modified architecture of Dadda Multiplier, and Imprecise 4-2 compressor, respectively. This is due to low logic-depth of the approximate compressors used in the proposed multipliers.

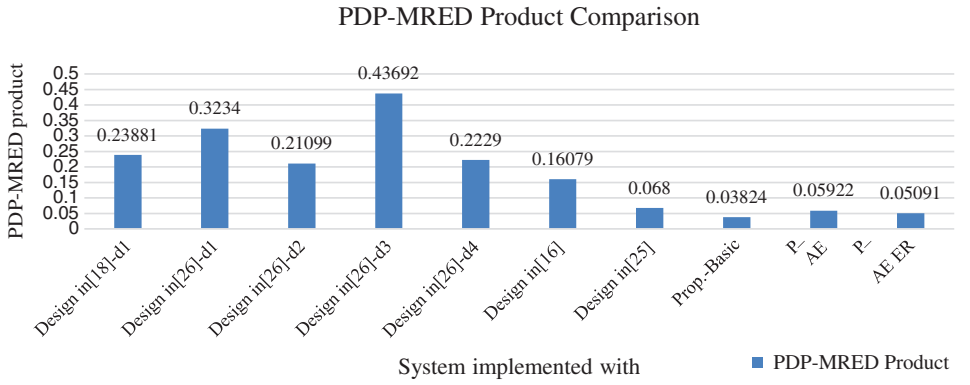
Table 4: Multipliers ($n = 8$) performance comparison

Multipliers	Power (μw)		Area ($\times 10^{-6}$ m^2)	Delay (ps)	PDP ($\times 10^{-13}$ Joules)	Maximum error	% Accuracy	PDPX error ($\times 10^{-11}$)
	Static	Total						
Exact	11.3	80.496	1415	5882	4.735	–	100	–
4-2CAM	7.23	49.788	1091	3689	1.837	512 (2^{n+1})	87.24	23.4
DQ4:2C1	5.67	40.085	861	3666	1.47	65,536 (2^{2n})	77.92	32.45
DQ4:2C2	6.14	44.280	942	3666	1.623	65,536 (2^{2n})	86.64	21.68
DQ4:2C3	7.09	52.892	1119	3755	1.986	65,536 (2^{2n})	77.76	44.17
DQ4:2C4	8.27	57.336	1200	3887	2.229	65,536 (2^{2n})	89.68	23
MADM	7.76	60.472	1221	3798	2.297	512 (2^{n+1})	93.48	14.97
I4-2C	10.8	76.8	1402	4673	3.589	512 (2^{n+1})	97.72	8.18
Proposed-basic	7.96	55.636	1364	3437	1.912	512 (2^{n+1})	97.62	4.55
P–AE	7.44	52.206	1248	3241	1.692	512 (2^{n+1})	97.34	4.5
P–AE ER	7.51	52.351	1263	3241	1.697	512 (2^{n+1})	97.46	4.3

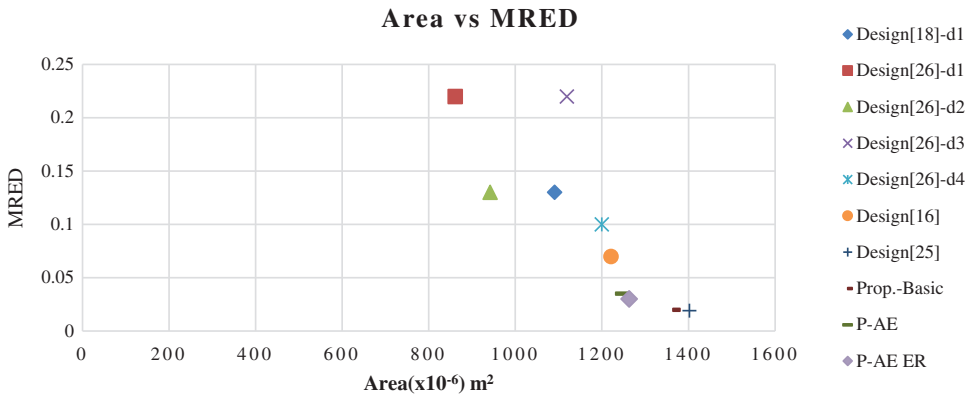
PDP of our basic, AE and AEER multipliers are 3.7%, 14.8%, 14.6%; 14.2%, 24.1%, 23.9%; 16.8%, 26.3%, 26.1%, and 46.7%, 52.9%, 52.7% improved compared to multipliers DQ4:2C3, DQ4:2C4, Modified architecture of Dadda Multiplier, and Imprecise 4-2 compressor, respectively. Nevertheless, designs in DQ4:2C1 and DQ4:2C2 fair better PDP compared to proposed designs, while the percentage of accuracy decreases. Effectiveness of the proposed and prior multipliers in optimizing Energy (PDP) and error is shown through PDP X Error metric in Tab. 4, and PDP-MRED product plot in Fig. 9a. It is noted from Tab. 4, to the least, the proposed designs demonstrates 80.6%, 85.9%, 79%, 89.7%, 80.2%, 69.6%, and 44.4% PDP X Error reduction compared to multipliers in 4-2 compressor-based approximate multiplier, DQ4:2C1, DQ4:2C2, DQ4:2C3, DQ4:2C4, Modified architecture of Dadda Multiplier, and Imprecise 4-2 compressor, respectively. Also note from Fig. 9a, that the Proposed-basic, P-AE and P-AEER multipliers demonstrates 44.1%, 13.2% and 26.5% PDP-MRED product reduction compared to the best approximate design compared.

Area cost of the proposed designs is low compared to Exact, and design in Imprecise 4-2 compressor. Approximate multipliers in DQ4:2C1, DQ4:2C2, DQ4:2C3, DQ4:2C4 use approximate compressors in all PP columns, while approximate designs in 4-2 compressor-based approximate multiplierandModified architecture of Dadda Multiplier don't add error compensation bias for X4X3X2X1 = "1111" in the exact part, and hence exhibit low area compared to the proposed designs. However, the average error of

designs in DQ4:2C1, DQ4:2C2, DQ4:2C3, DQ4:2C4, 4-2 compressor-based approximate multiplier, and Modified architecture of Dadda Multiplier are significantly high. Additionally, Note from Fig. 9b; the proposed multipliers demonstrate low MRED and high area while multiplier in DQ4:2C1 reveal low area and high MRED. Approximate designs in DQ4:2C2 and 4-2 compressor-based approximate multiplierexhibit moderate MRED and area among all other multipliers compared. Furthermore, Tab. 5 gives a brief comparison of power, delay, area, and PDP metrics of proposed multipliers for n = 8, 12, 16. It is noted from Tab. 5 that the power dissipation and area increases at 6X and 4.8X proportion for 2X increase in input operand bit-width.



(a)



(b)

Figure 9: Approximate multipliers (prior) comparison with the proposed multiplier (a) PDP-MRED product (b) Area *vs*. MRED

5 Implementation in Digital Image Processing

An implementation in image enhancement viz., smoothing & scaling, and signal processing applications is done in FPGA board to justify the novelty of modified multipliers in fault-tolerant image processing applications. The Verilog HDL models of the modified new variant multipliers and futuristic approximate designs defined in the literature are synthesized using Xilinx ISE 14.2 tool, and the prototype model for the application system is made by using Spartan 6 FPGA (XC6XLX45-CSG324 device). Input images and signals are send to the FPGA Board using Xilinx-MATLAB co-simulation with System Generator tool.

Table 5: Area, power, delay comparison of proposed multipliers for various input bits *(n)*

Parameter	n = 8			n = 12			n = 16		
	Proposed-basic	P-AE	P–AEER	Proposed-basic	P-AE	P–AE ER	Proposed-basic	P-AE	P–AE ER
Power ($\times 10^{-6}$w)	55.64	52.21	52.35	172.8	168.9	173.87	350.3	340.4	342.3
Delay (ns)	3.44	3.24	3.24	5.18	4.88	4.95	8.808	8.246	8.246
Area (μm^2)	1364	1248	1263	3436	3316	3356	6587	6348	6381
PDP ($\times 10^{-15}$ J)	191.4	169.16	169.61	895.1	824.23	860.7	3086.14	2806.93	2822.6
EDP (X 10^{-24} J)	658.4	548.1	549.5	4636.6	4022.2	4260.5	27188.9	23016.8	23145.3

5.1 Image Smoothing

In the digital images, Image smoothing technique is performed to reduce the blurring effect and noise. It is a pre-processing operation performed on images prior to the main object extraction. The smoothing operation performs averaging on the pixel intensity values of the input image in a pre-defined window and replaces the processing pixel with the result. The weight of the pixel in the window considered for smoothing operation depends on the type of mask used. For example, filter with 3 × 3 mask replace processing pixel with intensity value *G (x, y)* defined by

$$\begin{aligned} G(x,y) = {} & \alpha_1 * f(x-1,y-1) + \alpha_2 * f(x,y-1) + \alpha_3 * f(x-1,y+1) + \alpha_4 * f(x,y-1) \\ & + \alpha_5 * f(x,y) + \alpha_6 * f(x,y+1) + \alpha_7 * f(x-1,y+1) + \alpha_8 * f(x,y+1) \\ & + \alpha_9 * f(x+1,y+1) \end{aligned} \tag{17}$$

where $f(x \pm s, y \pm t)$ represents the pixel intensity values of the input image in the window. *s, t* can take values 0 or 1, and α_i represents the corresponding weights in the filter mask. The window is moved pixel by pixel till all the pixels in the input image are processed.

Fig. 10 shows the output processed images of the output by the image smoothing system performed along with new variant and other previous tabulated imprecise multipliers. The quality metrics Mean Absolute Error (MAE), Peak Signal to Noise Ratio (PSNR), and Structural Similarity Index (SSIM) [37] are used as measures to evaluate the operation of proposed approximate designs. It is estimated using output images processed by the smoothing system designed with error-tolerant and exact multipliers. MAE PSNR and MSE are defined by Eqs. (18)–(20).

$$MAE = 1/ab \sum_{x=0}^{a-1} \sum_{y=0}^{b-1} |G(x,y) - G'(x,y)| \tag{18}$$

$$PSNR = 20 \log \frac{255}{\sqrt{MSE}} \tag{19}$$

where

$$MSE = \frac{1}{ab} \sum_{x=0}^{a-1} \sum_{y=0}^{b-1} [G(x,y) - G'(x,y)]\text{^}2 \tag{20}$$

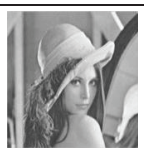
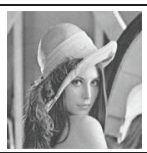
					
Standard input	*10% ND input image*	*20% ND input image*			
	(a)				
Image smoothing system with	***Output images-Lena***				
Exact Multiplier					
Accuracy-Configurable Adder(ACA)			parallel CMOS multipliers		
	MAE=376;PSNR=36.0412 ; SSIM=0.9069	*MAE=384;PSNR=35.5 36; SSIM=0.8982*		*MAE=930;PSNR= 32.772; SSIM=0.7391*	*MAE=942;PSNR= 32.54; SSIM=0.7278*
Parallel CMOS multipliers with improved 3:2 compressors			parallel CMOS multipliers		
	MAE=442;PSNR=34.964; SSIM=0.8699	*MAE=467;PSNR=34.3 943;SSIM=0.8478*		*MAE=439;PSNR= 35.398;SSIM=0.88 91*	*MAE=448;PSNR= 35.05;SSIM=0.87 98*
Parallel CMOS multipliers with improved 4:2 compressors			hybrid approximate adders		
	MAE=988;PSNR=32.657; SSIM=0.7293	*MAE=992;PSNR=31.9 75; SSIM=0.7165*		*MAE=344;PSNR= 37.625; SSIM=0.9186*	*MAE=362;PSNR= 37.257; SSIM=0.9190*
Wallace tree multiplier			*Proposed-basic*		
	MAE=132;PSNR=41.41: SSIM=0.9929	*MAE=148;PSNR=40.6 29: SSIM=0.9894*		*MAE=145.5; PSNR=41.034: SSIM=0.9921*	*MAE=150.5; PSNR=40.353: SSIM=0.9887*
P- AE			*P-AEER*		
	MAE=156.2;PSNR=39.01: SSIM=0.9842	*MAE=162.3;PSNR=38. 986: SSIM=0.9814*		*MAE=152.6;PSNR =39.812: SSIM=0.9903*	*MAE=157.2;PSN R=39.621: SSIM=0.9824*

Figure 10: (a) Image of input (b)–(g) Images of output processed with various multipliers for ND = 10% & 20%

$G(x, y)$ and $G'(x, y)$ indicate the image size of the output of the exact and error-tolerant system outputs, a and b. Note that, from Fig. 10, PSNR, MAE, and SSIM output image values are processed by image smoothing system with proposed multipliers–basic, P-AE, P-AE ER designs are more appreciable while comparing approximate multipliers in 4-2 compressor-based approximate multiplier, DQ4:2C1, DQ4:2C2, DQ4:2C3, DQ4:2C4 and Modified architecture of Dadda Multiplier based systems. This is due to the low average error performance of the proposed designs due to faithful approximation. Additionally, we have extracted Average MAE (AMAE) metric using different output images processed by a smoothing system with different standard input images - Lena, Boat, Cameraman, Bridge, Peppers, and shown in Fig. 11. Also by means of Fig. 11, AMAE output image values are processed by proposed-basic, P-AE and P-AE ER designs based systems are significantly better compared to approximate multipliers 4-2 compressor-based approximate multiplier, DQ4:2C1, DQ4:2C2, DQ4:2C3, DQ4:2C4 and Modified architecture of Dadda Multiplierbased systems. AMAE value of approximate multiplier based system fair better compared to the proposed technique and other approximate multiplier systems; however, it exhibits a high area. Also, it is noted that image smoothing system with proposed designs fairs better area compared to systems with designs in Modified architecture of Dadda Multiplier, Imprecise 4-2 compressor and conversely, it is higher when compared to systems with approximate multipliers in 4-2 compressor-based approximate multiplier, DQ4:2C1, DQ4:2C2, DQ4:2C3 and DQ4:2C4.P-AE and P-AEER based smoothing systems fair better processing delay compared to Proposed-basic,Modified architecture of Dadda Multiplier, DQ4:2C3, DQ4:2C4, 4-2 compressor-based approximate multiplier, and Imprecise 4-2 compressor built systems. Imprecise 4-2 compressor based system demonstrates the highest area and processing delay compared to related approximate multiplier smoothing systems.

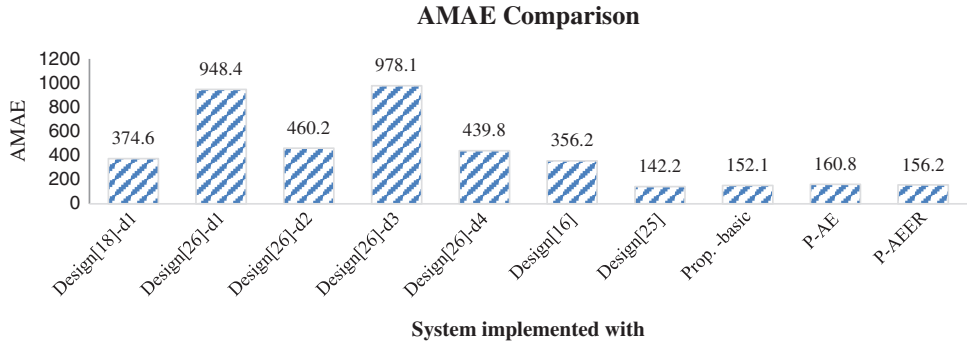


Figure 11: AMAE Comparison of output images with various multipliers

5.2 ECG Signal Processing

As implementation of 27 tap Finite impulse Response is done to check the functionality of proposed multiplier. Fig. 12 shows the Data Flow Graph (DFG) of n tap FIR filter. From Fig. 12 it is noted that the multiplier is the significant element that contributes towards the area and critical delay of the FIR filter. Coefficients for the FIR filter are chosen in MATLAB using the Remeez commands. An ECG signal is added and it is fed as an input to the FIR Filter. The processed output signals of the FIR filter implemented with new variant and tabulated previously developed approximate multipliers are measured with standard output to measure the accuracy efficacy of proposed multipliers. The I/O signals processed by the FIR filter designed with various multipliers are illustrated in Figs. 13a–13c. Note from Fig. 13c shows that the output waves.

Processed by Proposed-basic and FIR filters (P-AE based) have small deviations when compared with standard output. Output waves processed by Q4:2C1 and 4-2 compressor-based approximate multiplier FIR systems display the highest and moderate deviations, respectively, compared to the standard output.

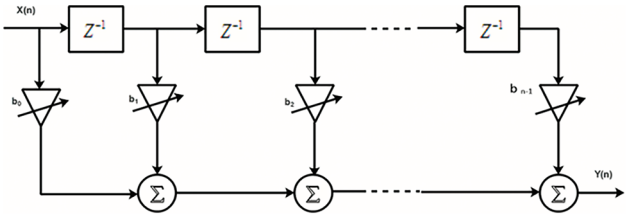
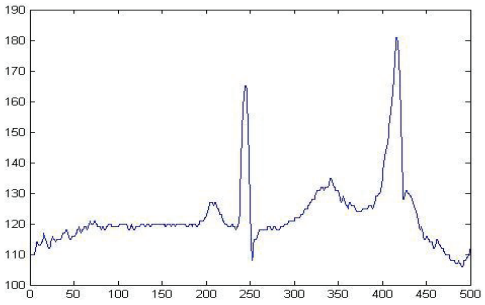
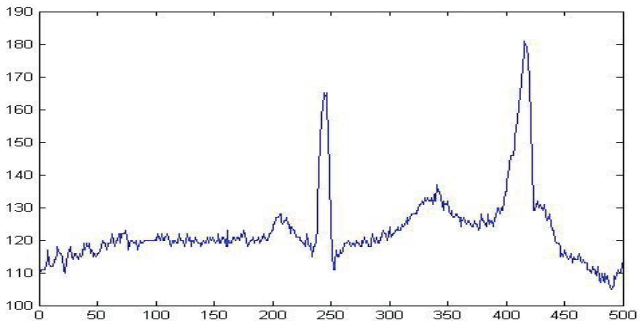


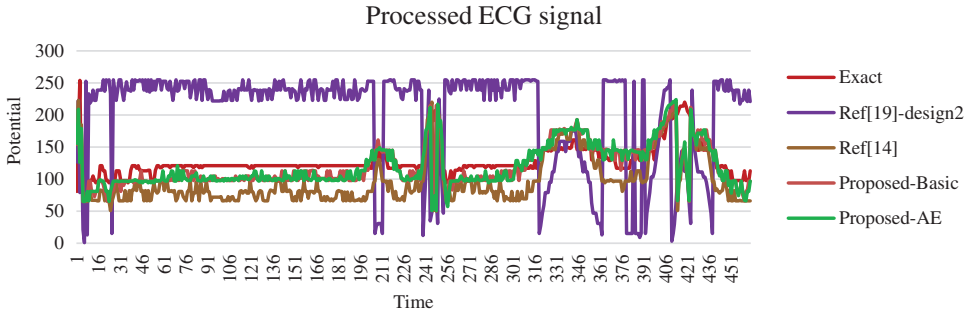
Figure 12: DFG of FIR filter



(a)



(b)



(c)

Figure 13: (a) Standard ECG input signal (b) ECG signal corrupted by white gaussian noise (c) Output signals processed by FIR filter systems

6 Conclusion

In the proposed research work, two area-efficient variants of 4:2 compressors (approximate type) targeted in the multiplier using PP compression. The logic of compressors is realized such that the designs generate sum without error in the first variant and carry without error in the second variant. Evaluations revealed that the proposed compressors fair better with regard to gate count and error reductions while comparing with the previous variants discussed in literature. Implementation of the new variant compressors in the Dadda multiplier disclosed the superior performance of the proposed multiplier with regard to processing speed and accuracy when compared to earlier designs. Enhanced variants of the proposed multiplier in terms of area and error recovery demonstrated better efficacy in terms of area at a trade-off in accuracy. Finally, the proposed multipliers are implemented in signal and image processing applications to verify the functionality and driving quality. Visual examination of processed output images and signals concluded that the proposed inexact multipliers perform similar to the standard design with minimal error deviation.

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Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

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