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Efficient Single-Stage Bridgeless AC to DC Converter Using Grey Wolf Optimization

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Abstract: Bridgeless single-stage converters are used for efficient (alternative current) AC-(direct current) DC conversion. These converters control generators, like electromagnetic meso- and micro-scale generators with low voltage. Power factor correction helps increase the factor of the power supply. The main advantage of the power factor is it shapes the input current for increasing the real power of the AC supply. In this paper, a two-switch bridgeless rectifier topology is designed with a power factor correction capability. For the proposed converter topology to have good power quality parameters, the closed loop scheme, which uses the grey wolf optimization (GWO) algorithm, is implemented. The successes of GWO encourage this research to implement GWO in the topology. The performance of the proposed topology is analyzed under different load conditions. Simulation is carried out using the MATLAB/Simulink environment, and the results are compared with those of conventional (proportional integral derivative) PID and (particle swarm optimization) PSO controllers. To validate the simulation results, a 350-W hardware prototype is implemented, and the voltage ripple, efficiency, and power factor under different load conditions are analyzed and tabulated. The comparative study clearly indicates that the proposed converter topology with a closed loop control scheme using the GWO algorithm improves the power factor to 0.9732 and reduces the voltage ripple to 0.12% with a conversion efficiency of 98.25%.

Keywords: Bridgeless; AC converter; DC converter; GWO controller; power factor

1 Introduction

The rapid boom of renewable energy technologies has led to pollution-free power generation with reduced fuel consumption and that uses abundantly available natural resources. Though renewable energy sources have many advantages over conventional energy resources, the power quality problem arises while it is interconnected with the grid. To overcome power quality issues, passive filters were used along with power converters in olden days. However, this practice was discouraged due to additional stage requirement and the cost and over size of power conversion stages. In this paper, the power quality

problem is addressed while interconnecting the AC-DC converter with the grid. To achieve the objective of the proposed work, the researchers contributed many works to the literature.

A single-stage three-level isolated power factor corrected AC/DC converter was proposed for low power applications where switches are shared between stages [1]. In this work, the output voltage is regulated with input current shaping. To have a good power factor in line voltages, the switches are triggered using the (zero volt switching) ZVS and (zero current switching) ZCS concept. Having the same switches with different switching schemes enables single-stage conversion. The result reveals that the proposed converter could achieve a 0.99 power factor with 95.2% efficiency.

The proposed converter could improve the power factor during boost or buck converter mode charging. Due to power quality problems addressed in (switched-mode power supply) SMPS supplies to personal computer had led to usage of non-isolated power factor corrected converter used at the front end of (switched mode power converter) SMPC to resolve power quality issues. To select best operating mode of front-end converter, a simulation was carried out and same was implemented on experimental prototype. The results revealed that the proposed converter could overcome the conventional converter in terms of power factor, voltage regulation and harmonic content. A power conversion interface was introduced which consist of power factor correction stage and buck converter unit.

The rest of this paper is organized as follows. Section 2 presents the related literature on the proposed model. Section 3 briefly discusses the proposed technique. Section 4 presents the results and their evaluation, and Section 5 concludes the research work.

2 Literature Survey

A highly efficient soft-switched AC/DC converter, which incorporates the boost and buck converter topologies, was proposed by a previous study [2]. In the converter, the boost converter operates in discontinuous mode, ensuring power factor correction, while the buck converter operates to ensure a stable ripple-free regulated DC output voltage. This investigation concluded that the proposed concept could achieve 94.8% efficiency. 0.995 pf with 9.25%. For low power applications, an output voltage regulated with a power factor corrected AC/DC converter was proposed [3]. The loss-free resistor behavior was used in the (single-ended primary-inductor converter) SEPIC and the cuk converter to improve the power factor. To avoid distortion near the zero input current, a variable bandwidth hysteresis controller was used. The results indicate that the performance of the cuk converter is better than that of the SEPIC converter in terms of achieving the objective.

Without an input diode bridge, a single-stage dual output PFC SEPIC converter was proposed for the RMS voltage range of 85 V to 265 V [4]. To replace two individual inductors, a magnetically coupled inductor was introduced in the circuit. The proposed work could achieve 95% efficiency with a near-unity power factor and a (total harmonic distortion) THD of 14.8%. A continuous conduction mode (unified power format) UPF single-phase bridgeless buck rectifier was proposed in a previous study [5]. The proposed topology could achieve dead angle freedom at the zero crossing of the input current. A THD of less than 7% and a near-unity power factor with 94% maximum efficiency could be achieved.

An analysis was performed to explore the reason for the occurrence of high voltage stress in a single-stage power factor correction converter and provide a solution [6,7]. The previous works reported the reason under the steady state condition, but transient performance was not considered [8]. The inherent negative current feedback property in an output inductor causes voltage stress. Incorporating an auxiliary circuit into the main transformer could reduce the voltage stress during the output variation of load. A power-factor-corrected integrated battery charger was proposed for electric vehicle applications [9,10]. The charger could operate the power factor of more than 0.9 for both boost and buck operations at 48 or 192 V [11].

The multilevel AC/DC conversion stage was introduced due to low switching harmonics and with-stand capacity of passive components. The proposed conversion interface could achieve unity power factor and low harmonic distortion. For telecommunication applications, a three-level full bridge AC/DC converter was proposed and investigated by incorporating three different closed loops [12]. The results indicate that genetic-algorithm-based average current control performs better in terms of power factor, THD, and UPF without a filter requirement at the source side under disturbances in the source and load sides. A three-phase Vienna AC/DC converter with power factor correction in which (field-programmable gate array) FPGA-based emulation was implemented for generating switching pattern was proposed in a previous study [13]. In the proposed scheme, the control scheme was implemented by incorporating Hardware-in-the-Loop testing in the system, thereby increasing the accuracy. A semi-bridgeless boost rectifier was presented for power factor correction using a sliding mode controller [14]. The proposed topology consists of two boost cells operating in complementary mode. The third order harmonic component reportedly decreased. The problem raised due to two unbalanced inductors was also mitigated. To achieve high power density and efficiency, a three-level single-phase rectifier operating in one direction with the (power factor correction) PFC was presented by a previous study [15]. This topology exhibits a lower switching loss than the state of the art; the low conduction loss results in 98% maximum efficiency with 2.18% THD at 140 kHz switching frequency. A single-stage AC/DC converter was proposed with ZVS capability in all active switches [16]. The H-bridge topology was used, offering power factor correction and DC output voltage regulation. The proposed scheme could achieve 92% maximum efficiency due to the reduced losses in the magnetic reactor and transformer.

For power quality improvement, AC to DC converters were proposed on the basis of the magnetic energy recovery switch [17]. The proposed converter topology was used in high-current and low-voltage applications, such as electric vehicle charging. The proposed converter can maintain good power quality parameters in the presence of source and load disturbances, and the power factor was maintained at 0.99 with R and RL loads. To drive a (brushless DC electric motor) BLDC motor, a new AC/DC converter topology was proposed in combination with the chopper circuit, allowing the voltage boosting during discontinuous conduction and reduction during the continuous mode of operation [18].

The proposed converter has only one switch, which could supply the required real power with an improved power factor at 25 kHz switching frequency. For the BLDC motor to drive with an improved power factor, the Luo converter was proposed on the basis of single voltage sensor [19]. It was able to provide good power quality parameters with values consistent with the IEC 61000–3–2 standard with unity power factor. A forward converter capable of ZVS switching with power factor correction for the split-phase charger was proposed by a study [20]. Given the soft switching of active switches, the converter efficiency improved considerably with good power quality indices. The proposed converter was simulated and built in a lab for checking the feasibility on a real test bench, achieving the maximum efficiency of 94% with a power of 0.985.

3 Proposed GWO-Based Converter Topology

The proposed converter topology consists of two active swiches, S_1 and S_2, which are switched asymmetrcally as shown in the figure, which also shows no continous conduction. The switches are triggered as per the switching pattern generated and shown in Fig. 1. The pulses are generated using the phase shifted carrier (pulse with modulation) PWM technique, which reduces the switching frequency in the individual leg, and the switching angle is distributed among the switches. The rectifier bridge consist of diodes D_1–D_4, which assist the main switches in both the negative and postive half cycles. Inductors L_1 and L_2 are placed in the upper and lower arms, respectively. The load voltage is shared by capacitors C_1 and C_2.

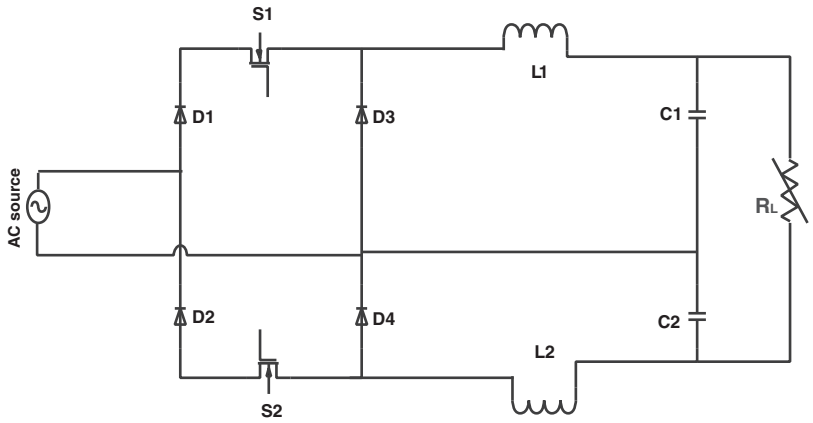

Figure 1: Proposed converter topology

3.1 Modes of Operation

Mode 1: In this mode, switch S1 is turned on, the current conduction path is shown in Fig. 2a, and the load voltage is being shared among the capacitors.

$$V_{L1} = V_{in} - V_{o1} \tag{1}$$

$$V_{01} = \frac{1}{C_1}\int_{t_o}^{t_1} i^I + V_{C1}(t_o) \tag{2}$$

Mode 2: At the end of Mode 1, switch S1 is turned off and switch S2 is turned on. The corresponding current path is shown in Fig. 2b. During this mode, diodes D2 and D4 assist the current conduction. Both inductors are charging in this mode.

$$V_{L2} = V_{in} - V_{o2} \tag{3}$$

$$V_{02} = \frac{1}{C_2}\int_{t_1}^{t_2} i^{II} + V_{C2}(t_1) \tag{4}$$

$$V_o = V_{o1} + V_{o2} \tag{5}$$

$$I_{in}(peak) = \frac{\sqrt{2}P_o}{V_{in}} \tag{6}$$

$$I_{sw} = \frac{\sqrt{2}P_o}{f_s * V_{in}} \tag{7}$$

V_{o1} and V_{o2} are the voltages across output capacitors C_1 and C_2, respectively; V_{in} is the input RMS voltage; P_o is the output power; and f_s is the switching frequency.

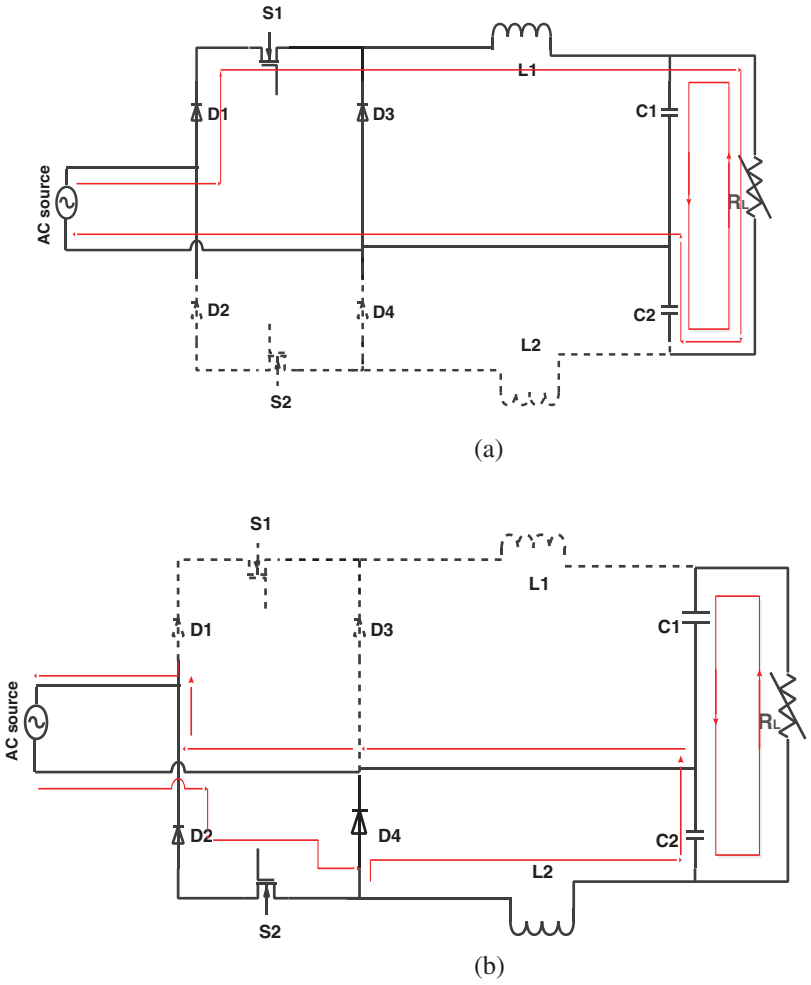

Figure 2: (a) Mode 1 (b) Mode 2

3.2 Design of Proposed Converter

Design of inductor L_1, L_2: The inductor values are assumed equal, that is, $L = L_1 = L_2$, and the zero crossing dead angle zero. The inductor value can be determined using the following equation, where ΔI_L indicates the input current ripple, and V_{c1} indicates the voltage across output capacitor C1.

$$L = \frac{\sqrt{2} V_{in} * D_{min}}{\Delta I_L * f_1} \tag{8}$$

$$D_{min} = \frac{V_{C1}}{V_{C1} + V_{in,max}} \tag{9}$$

Design of output capacitor C_1, C_2: The output capacitor value is calculated using the following equation, assuming unity power factor. The voltage ripple is approximately equal to the difference between the input RMS voltage and the average output voltage regardless of the circuit topology. Fig. 3 shows that the theoretical key wave form of the propsoed system. V_{in} and I_{in} indicate the input RMS voltage, f_1 indicates the supply frequency, and ΔV_{out} indicates the voltage ripple.

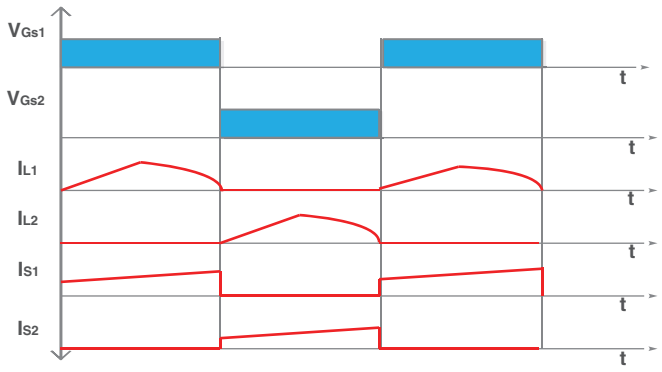

Figure 3: Theoretical key waveform

$$\text{Pin} = 2\ \text{V}_{\text{in}}\text{I}_{\text{in}}\sin^2\omega t \tag{10}$$

$$\omega = 2\pi f_1 \tag{11}$$

$$C_{out} = \frac{P_{out}}{\Delta V_{out} * V_{out} * \omega} \tag{12}$$

3.3 Grey Wolf Optimization

Researchers have been using meta-heuristic algorithms in the last decades because of their simplicity and flexibility in solving non-linear problems and they need no derivative concepts and avoid local minima [21]. To overcome the drawbacks of well-known nature-inspired algorithms, such as genetic algorithm, gravitational search algorithm, and differential evolution, a new algorithm called grey wolf optimization (GWO) was proposed by Seyedali Mirjalili. GWO is inspired by the leadership and hunting behavior of wolves and their hierarchy in handling preys. To depict the encircling of a prey by wolves, the following mathematical model was established:

$$\vec{d} = |\vec{c}.\overrightarrow{X_p}(t) - \vec{X}(t)|, \tag{13}$$

$$\vec{X}(t+1) = \overrightarrow{X_p}(t) - \vec{a}\vec{d}, \tag{14}$$

where $\overrightarrow{X_p}(t)$ indicates the position vector of the prey, $\vec{X}(t)$ indicates the position of the wolf, vectors $\vec{a}, \overrightarrow{c}$ are the coefficient vectors.

$$\vec{a} = 2\epsilon\overrightarrow{r_1} - \varepsilon \tag{15}$$

$$\vec{c} = 2\overrightarrow{r_2} \tag{16}$$

ε is linearly decreasing from 2 to 0 in the interval of iteration, and $\overrightarrow{r_1}$, $\overrightarrow{r_2}$ −are the random vectors in the interval of [0,1].

To imitate the hunting behavior of wolves, the following mathematical expressions were established.

$$\overrightarrow{D_\alpha} = |\overrightarrow{c_1}\overrightarrow{X_\alpha} - \vec{X}| \tag{17}$$

$$\overrightarrow{D_\beta} = |\overrightarrow{c_2}\overrightarrow{X_\beta} - \vec{X}| \tag{18}$$

$$\overrightarrow{D_\delta} = |\overrightarrow{c_3}\overrightarrow{X_\delta} - \vec{X}| \tag{19}$$

$$\overrightarrow{X_1} = \overrightarrow{X_\alpha} - \overrightarrow{a_1}\overrightarrow{D_\alpha} \tag{20}$$

$$\overrightarrow{X_2} = \overrightarrow{X_\beta} - \overrightarrow{a_2}\overrightarrow{D_\beta} \tag{21}$$

$$\overrightarrow{X_3} = \overrightarrow{X_\delta} - \overrightarrow{a_1}\overrightarrow{D_\delta} \tag{22}$$

$$\vec{X}(t+1) = \frac{\overrightarrow{(X_1} + \overrightarrow{X_2} + \overrightarrow{X_2})}{3} \tag{23}$$

The next phase involves the exploitation and exploration of the prey. The wolves start attacking the prey when no movement is noted in the prey. To imitate this behavior, the value of ε is linearly decreased from 2 to 0. The wolves are instructed to attack the prey if $|\vec{a}|$ is less than one; otherwise, the wolves keep on searching the prey.

4 Simulation Results

The proposed converter is simulated in the MATLAB/Simulink environment to analyze the performance of the converter using the circuit parameters listed in Tab. 2. The active switches are symmetrically triggered. The switching pattern is generated using the phase shifted carrier PWM (phase-shifted carrier pulse width modulation based) PSCPWM technique in which the switching angle is distributed to reduce the frequency. The switching pattern using the PSCPWM technique is shown in Fig. 4. The input voltage applied is 230 V AC, and the output voltage obtained is 160.5 V with a 0.12% ripple content. The source voltage, output voltage, source current, and output current waveforms are shown in Fig. 5. The conventional PID controller without a tuning gain was implemented initially, and the results are compared with those of the PSO and proposed meta-heuristic GWO controllers. Tab. 2 clearly shows that the gain tuned by the GWO controller yielded a better performance than the other two methods. The source current had a total harmonic distortion of 4.45% when delivering real power of 340.5 W and reactive power of 15.1 KVAR. The power factor of the proposed converter drastically increased to 0.9732, which is near unity, resulting in a conversion efficiency of 98.25%.

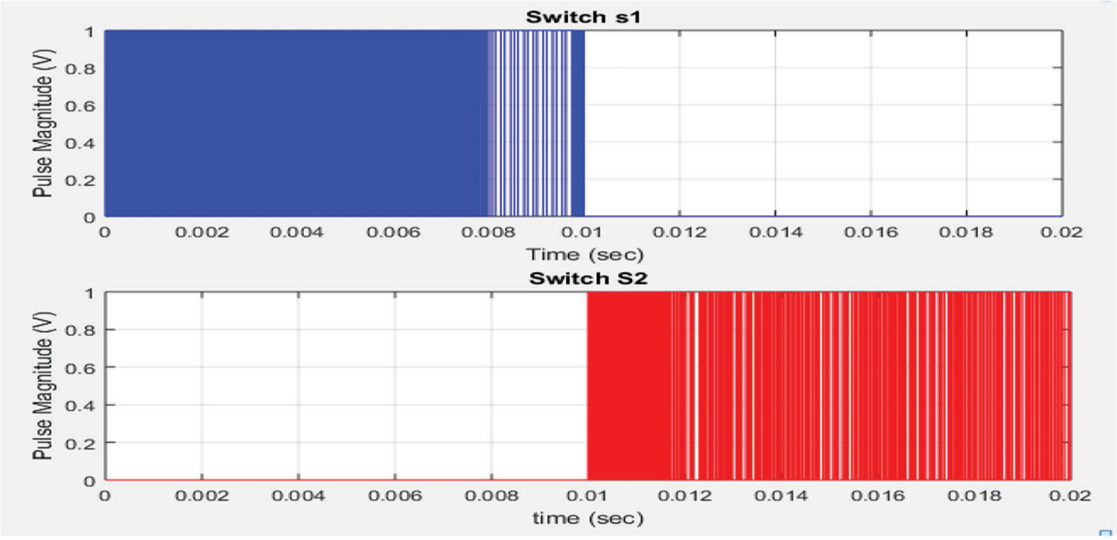

Figure 4: Switching pattern generated for switches S1 and S2

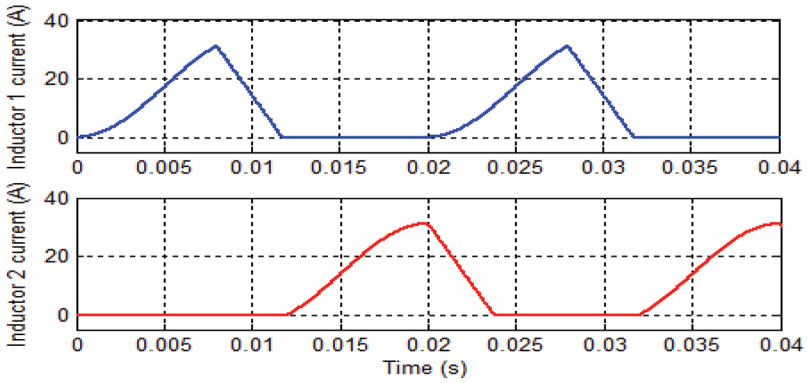

Figure 5: Inductor current IL1, IL2

Fig. 6 indicates that the proposed converter delivers more output power with high conversion efficiency when the GWO controller is used to tune the PID controller gain than when the PSO controller is used.

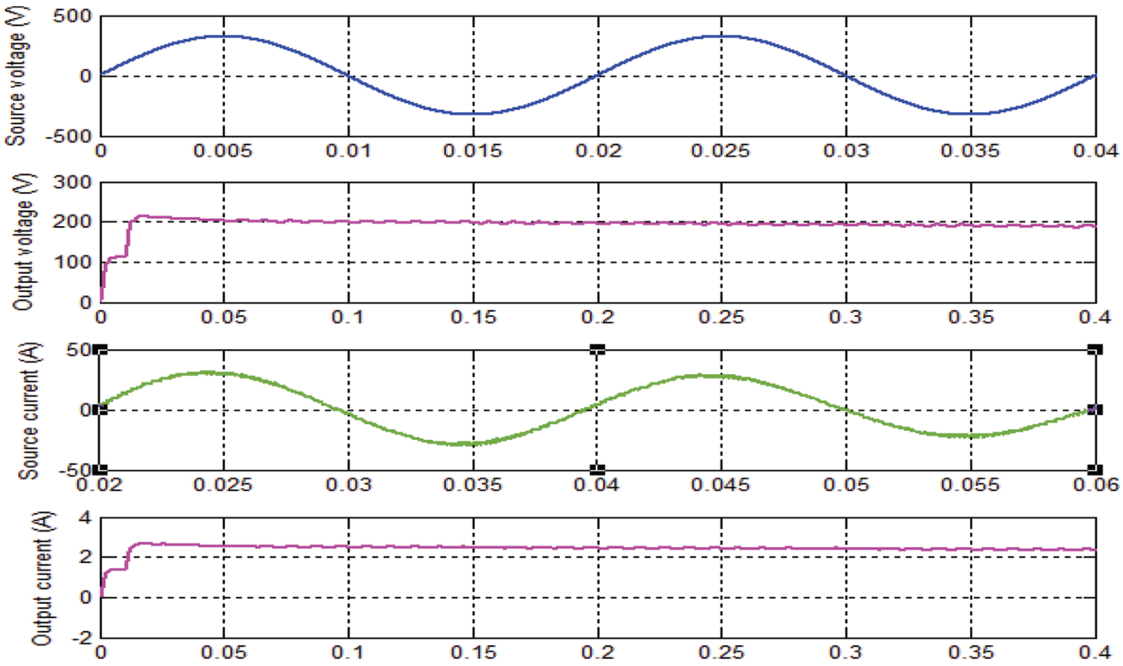

Figure 6: Source voltage, output current, source current, and output current

4.1 Performance Comparison

The performance comparison between the PID controller without gain tuning, the PSO controller, and the GWO controller is presented in Tab. 1. The source current THD window of the PID controller without gain tuning, the PSO controller, and the GWO controller is shown in Figs. 7 and 8. From the source current, the THD of the PID controller is reduced compared to those of the other two methods.

Table 1: Performance comparison

S. No	Parameter	Without tuning PID controller	PSO-algorithm-based controller	GWO-algorithm-based controller
1	Output voltage	190 V	195 V	200 V
2	Input voltage	230 V AC	230 V AC	230 V AC
3	Power factor	0.8922	0.9123	0.9732
4	Voltage ripple	0.28%	0.18%	0.12%
5	Source current THD	9.31%	7.24%	4.45%
6	Efficiency	0.9016	0.9124	0.9825
7	Real power	339.2 W	340.2 W	340.5W
8	Reactive power	14.92 kVAR	14.92 kVAR	15.1 kVAR

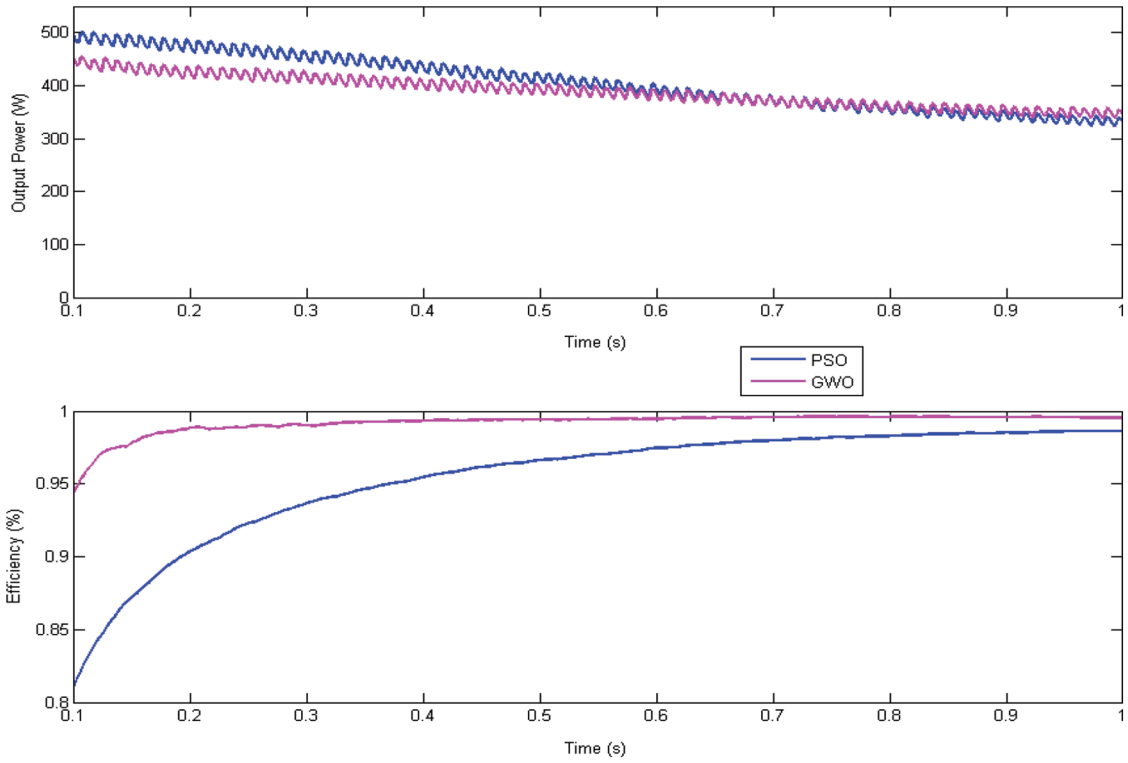

Figure 7: Output power and efficiency with respect to time

4.2 Experimental Results

To validate the simulation results on a real test bench, the proposed 350 W–200 V topology with 20 kHZ switching frequency was constructed using the circuit components listed in Tab. 1. The performance of the proposed converter topology with a GWO controller is compared under different values of the load resistance connected to the output port. Tab. 2 indicates that the proposed rectifier can achieve 97.15% maximum efficiency at full load condition with a power factor of 0.9732, which is near unity.

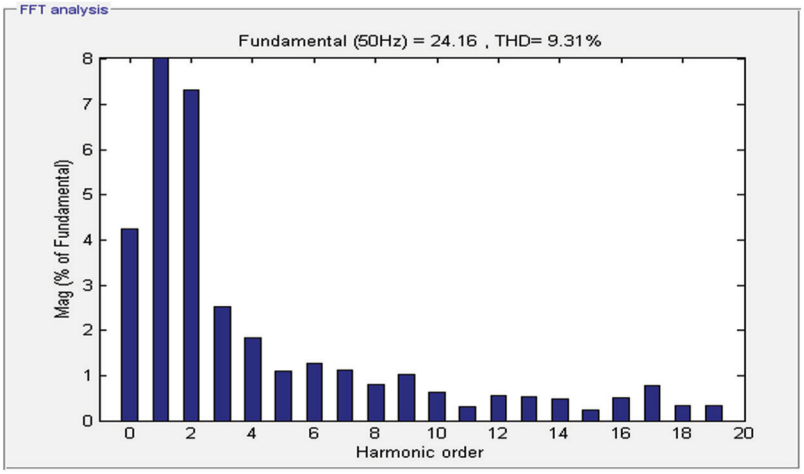

Figure 8: THD window of source current without tuning PID controller

Table 2: Hardware performance comparison

S. No	Controller	Parameter	25% of load	50% of load	75% of load	100% of load
1	PID controller without tuning	Voltage ripple	0.32%	0.25%	0.25%	0.28%
		Efficiency	0.8925%	0.9012%	0.9016%	0.9016%
		Power factor	0.8922	0.8922	0.8922	0.8922
2	PSO-algorithm-based controller	Voltage ripple	0.28%	0.15%	0.14%	0.18%
		Efficiency	0.9011%	0.9065%	0.9098%	0.9124%
		Power factor	0.9123	0.9123	0.9123	0.9123
3	GWO-algorithm-based controller	Voltage ripple	0.17%	0.15%	0.15%	0.23%
		Efficiency	0.9525%	0.9455%	0.9625%	0.9715%
		Power factor	0.9732	0.9732	0.9732	0.9722

4.3 Hardware Performance Comparison

The power quality parameters listed in Tab. 2 were measured using a TEKTRONIX (SMU 2450) power analyzer. The measured efficiency was 97.15%, which agrees with the simulation efficiency. The switches were triggered at 20 kHz frequency, and the pulses generated are shown in Fig. 9. The measured input voltage of 230 V AC and the current of 2.5A are shown in Fig. 10. The measured inductor current is shown in Fig. 11. The input voltage and current waveform is shown in Fig. 12. The experimental output voltage obtained was 195 V, which is near the simulation result with a 0.5% voltage ripple.

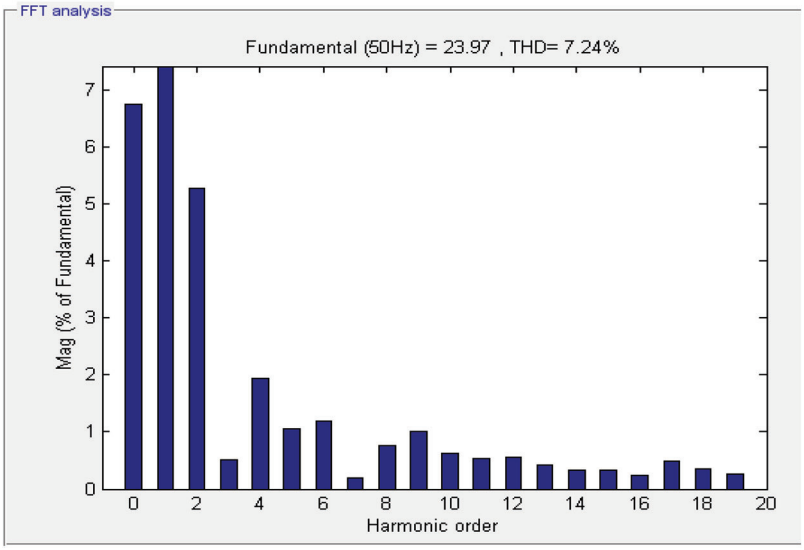

Figure 9: THD window of source current with PSO controller

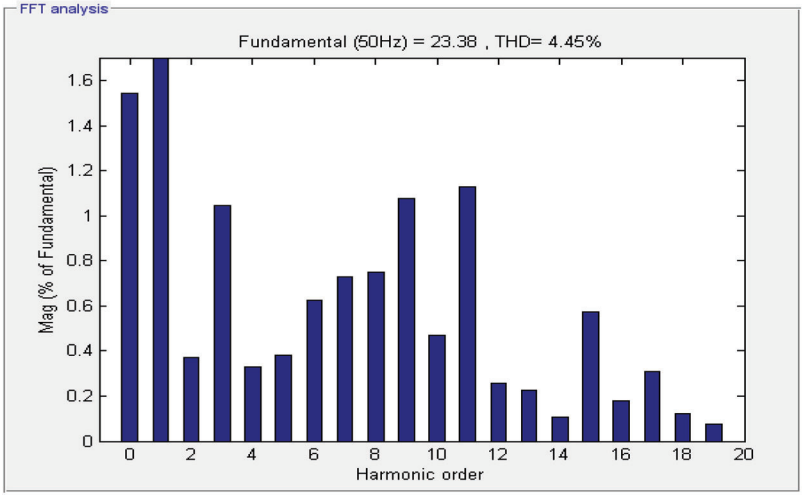

Figure 10: THD window of source current with GWO controller

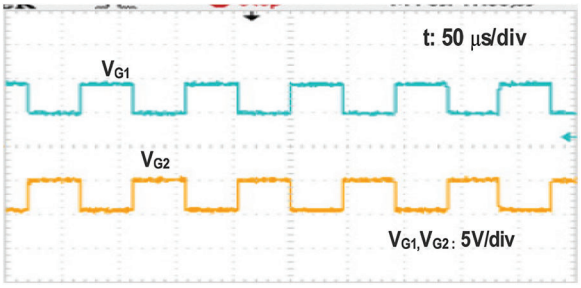

Figure 11: Gate pulses applied to switch S_1, S_2

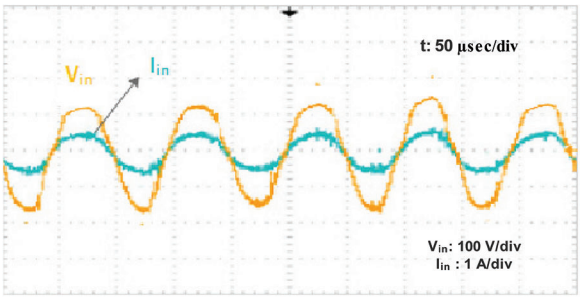

Figure 12: Input voltage and current

5 Conclusions

A highly efficient bridgeless AC/DC converter with a topology capable of power factor correction is proposed with a GWO0-based closed loop control scheme. The detailed analysis of the proposed topology and the design of the circuit parameters were discussed. Simulation was carried out using MATLAB/Simulink to analyze the power quality parameters of the proposed topology, and the results were compared with those of the conventional and PSO controllers. The prototype hardware of 350 W was implemented in the laboratory under various load conditions. The power quality parameters of the proposed scheme, like voltage ripple, power factor, source current THD, and efficiency, under different load conditions are better than those of the other two closed loop control schemes. In the future, the firefly and butterfly optimization techniques of swarm intelligence can be tested and the power coversion can improved.

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Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

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