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Design and Analysis of 4-bit 1.2GS/s Low Power CMOS Clocked Flash ADC

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Abstract: High-quality, high-resolution flash ADCs are used in reliable VLSI (Very Large-Scale Integrated) circuits to minimize the power consumption. An analogue electrical signal is converted into a discrete-valued sequence by these ADCs. This paper proposes a four-bit 1.2GS/s low-power Clocked Flash ADC (C-FADC). A low-power Clocked-Improved Threshold Inverter Quantization (CITIQ) comparator, an Adaptive Bubble Free (ABF) logic circuit, and a compact Binary Encoder (BE) are all part of the presented structure. A clock network in the comparator circuit reduces skew and jitters, while an ABF logic circuit detects and corrects fourth order bubble faults detected from thermometer code, and then the BE transforms the bubble free code into binary code. A Tanner EDA with 250-nm Technology is used to implement the C-FADC. The proposed design achieves ENOB of 3.56, uses 3.24 mW of power, and has a FOM of 0.274pJ/conv.-step at an input frequency of 85 MHz. The suggested C-FADC has differential and integral nonlinearities of ±0.65 LSB and +0.45/-0.5 LSB, respectively.

Keywords: Skew and jitter; offset voltage; clock network; adaptive bubble free logic

1 Introduction

In recent days, ADC has become a critical component in a wide range of applications, including satellite communication, instrumentation and measurement, industrial automation, defence, and aerospace applications, among others. Low-power, low-energy, high-speed, and high-resolution ADCs are needed for these applications. Analog signals are mostly present in nature, and they must be converted to digital signals. As a result, ADC is preferred for converting Analog to Digital signals. Over current ADCs such as Successive Approximation ADC, Sigma-Delta ADC, Dual Slope converters, Sub-ranges and two-step ADC, interpolating and folding ADC, FADC is often used for extreme speed requests. Because of its simple architecture, parallel operation, and non-linearity, the Flash ADC [1] was chosen. It makes use of a comparator, and the TH2B (Thermometer to Binary) encoder is an essential part of the digital conversion process. The resolution is directly proportional to the necessity of comparators. Because of the increased number of comparators, this method has a major drawback in that its construction, power utilization and structure area. The resolution quality decreases as the number of comparators decreases. As a result, there is a trade-off between the area and the quality of the resolution [2]. A parallel link of

2^N-1 comparators is needed to design an N-bit FADC [3] with high-resolution quality. It takes an analogue voltage signal (V_{in}) as input and compares it to V_{ref} using comparators. To get maximum output voltage swing, the comparator output signals are added to the gain boosters. The thermometer code is the response of gain boosters. If the value one is shown above zero in a thermometer code, a bubble fault appears. By developing binary codes, these bubble faults are reduced. Several publications have recently published articles on research into lowering the power consumption of ADCs. Using multiple references and sequence initialization, this technique also achieves very low switching energy. However, the amount of power used to create the extra sub references limits its attraction. Both source information and digital logic circuits benefit from VLSI design because it reduces the circuit area, costs, and low power dissipation line regulation factors. To minimize area and power consumption while maintaining high-resolution efficiency, the proposed Clocked-Flash ADC employs a comparator based on Clocked Improved Threshold Inverter Quantization (CITIQ), an Adaptive Bubble Free (ABF) logic circuit, and a Binary Encoder (BE). Two cascaded inverters and a dual collection of NMOS and PMOS transistors make up the CITIQ comparator. To correct bubble faults, a binary encoder is coupled with an ABF logic circuit, which is then used to code the maximum inputs into a minimum output. With an input signal frequency of 85 MHz, the presented 4-bit C-FADC core achieves a 23.2 dB signal to noise distortion ratio. This proposed architecture is expected to produce 3.56 Effective Number of Bits (ENOB) at 1.2 GS/s. Due to the Virtual Resolution Bandwidth (VRB) of 500 MHz, the C-FADC consumes 3.24 mW power and has a figure of merit is 0.274 pJ/con.-step with a 1.4 V supply.

This paper is organized as follows: The section1 introduces FADC and its features. The study foundation is mentioned in Section 2. Section 3 proposes a Clocked FADC built with the aid of a CITIQ comparator, an ABF, and a binary encoder. Graphical response and outcomes are given out in Section 4. Section 5 exhibits the concluding part.

2 Related Work

To endorse a broad input swing, the Flash ADC is optimized for 5-bit using multi-input logic gates [4]. The dynamic range of the input was determined by five input logic gates. It takes the threshold voltage, as a reference voltage and outputs Vdd/2 as the comparator's result. It is built a Flash ADC with a multiplexer-based encoder that is suitable for Ultra-Wide Band (UWB) applications [5]. By using an area-efficient MUX-based encoder, it decreases the amount of space and power used. The paper [6] discusses 3-bit TIQ, which is based on FADC. It is made up of a series of cascaded inverters. It does not require any additional input voltage because it optimizes the transistor aspect ratio to use the inverter switching potential as an input reference voltage. The linearity execution for a fixed input gate region was improved by nearly 30% using a well-characterized resistor averaging method [7]. The offset reductions caused by resistive averaging are reported as a part of the yield and are used to simulate resistor averaging. To achieve small in size, low-power, and fast A2D (Analog-to-Digital) converters, increase the process cycle variation in nano scale CMOS design [8]. A four-bit F-ADC built on 90nm technology will eliminate the need for a reference potential creation network. A 12-bit 180-nm CMOS technology is used to plan and execute a hybrid ADC [9], which combines the SAR and Flash ADCs to form a 2-step quantizer. A string of resistor DACs is also planned and executed. Because of the Flash architecture, this hybrid ADC is faster. Similarly, the power and resolution can be reduced by using the SAR structure. Pre-amplifiers [10] are placed in front of the comparator on a regular basis to increase comparative speed and reduce error. The precision of FADC is limited by the comparator with Preamplifiers due to random effects. The frequency cutoff ranges of MOSFETs are constantly increasing to reduce the size of CMOS technologies, results a linear increase in the transition speed of analog-to-digital converters [11]. However, in trendsetting technologies, the usable source voltage is closer to, or even less than, 1V, limiting the speed of traditional latch comparators. To reduce dynamic power consumption, a technique known as the

self-reset method [12] has been developed, which has been improved to achieve a shorter reset period. While the aforementioned techniques are effective in increasing the force productivity of low-potential comparators, they are unable to effectively upgrade the comparator's speed. The 6b/8b TIQ Flash ADC was designed using a dynamic programming approach [13], which included two techniques: Searching the data set efficiently when considering several paths, and modifying the layout of a data set to eliminate differential and integral non-linearity errors in order to choose the correct switching gate voltage. The start voltage, end voltage, area and connections are the limitations of this method. The technique of averaging is used to improve the linearity of a flash-type ADC beyond the single comparator matching limit. Many gain stages of the converter will use interpolation to reduce the size of the fore part of the amplifiers and the capacitance at the input side [14]. As compared to resistive installation the capacitive interpolation consumes low power, provides verifiable track-and-hold operation, and has no boundary impacts, resulting in an effective drive simple conversion interface. Since the circuit size is not negligible, RF design approaches that use EMF and simulation links design are needed for the highest conversion speed using advanced CMOS techniques [15]. As a result, this circuit needs careful attention to its feature and bandwidth for sampling the analogue signal in track and hold buffers, and Master-Slave (MS) flip-flops are used in comparators, but 10-GHz frequency circuits are extremely difficult to build. A low-potential bulk-driven based latch comparator structure [16] is proposed, which incline the mass hubs concept and sufficient potentials in the testing stage to lower their edge voltages, while setting the input information into the mass hubs during the contrast process to provide additional transconductance. To eliminate the effect of the bubble fault, the Flash ADC [17] employs the offset-cancellation process. However, this approach is ineffective at high resolution. As compared to multiple comparator techniques, the charge distribution latched dynamic comparator offers the lowest force delay product of 0.002fJ. A capacitive folding technique based on different calibration methods and a 5-bit Flash ADC [18] is designed to reduce threshold inaccuracies and folding errors in the transformation phase by lowering the comparison count. Dynamic folding logic allows for fast operation while also preventing charge leakage. A 4-bit 200 MS digital FADC with an ENOB of 3.5 and 23.3 SNDR is synthesized; it reduces design effort and has an ENOB of 3.5 with 23.3 SNDR [19]. In this work, a gate-based digital comparator is constructed using NAND-NOR logic, and encoder synthesized architecture is implemented. To diminish the unpredictability of simple limits and the necessary precision, the flash converter [20] combines digital rectification and an assignment. Low-impedance eliminates the need for an extremely precise resistor reference ladder, and the comparator execution is decoupled from coordinating requirements, allowing for the use of small and fast comparators.

The area, proficient structure known as a multiplexer pass gate encoder and low power comparator architecture is coordinated by the R-Flash ADC structure. The sensitivity of the elements used in the framework and its adaptation to fault tolerance can be used to determine the system reliability. If a problem is found in the redundant block, the bubble fault corrector recognizes the error and ensures the system [21]. The two phases of the clock (ON and OFF) operation is used in a time-dependent flash structured ADC [22]. This two-phase plan significantly reduces power consumption. The input capacitance in this work is kept to a minimum, and an on-chip adjustment circuit is used to suppress various mismatches. Previous research in flash ADC revealed a low-resolution quality as a result of converting the thermometer code to parallel code, which limits the speed and power. Clocked Flash ADC is suggested to address these limitations.

3 Proposed Clocked Flash ADC

The Flash (parallel) type ADC architecture is scrupulously used for high speed and low resolution applications. An analogue electrical signal is converted into binary coded output by a Clocked Flash ADC. The blocks involved in the C-Flash ADC is shown in Fig. 1. The Clocked Improved Threshold

Inverter Quantization (CITIQ) comparator, Adaptive Bubble Free (ABF) logic circuit, and Binary Encoder (BE) are three essential blocks in the Clocked Flash ADC. The flow chart depicted in Fig. 2. Illustrates the overall workflow of the proposed C-FADC. The comparator specification takes into account two essential factors. One is that when translating analogue signals to thermometer code, certain bubble faults can occur. Variations in fabrication parameters cause unusual impacts, resulting in a variety of offset potentials. As a result of these arbitrary impacts, relative offset potentials between adjoining comparators are formed, causing bubble fault. In an analogue comparator circuit, this comparator offset voltage may be considered, but it is ignored in the digital domain. In addition, the clock skew and jitters are shown in Fig. 3. Clock skew and jitter are influenced by environmental factors such as power supply and temperature. The skew is concerned with the output signal propagation delay. It is the propagation delay that causes variations in output signals. Race conditions and other timing errors caused by over the top skew, especially for clock signals, can result in framework data faults. Poor skew, in any case, will result in a slower most extreme framework speed, limiting framework efficiency. The primary cause of jitter in clock propagation is power supply variance, which degrades the dynamic parameter signal to noise ratio. To mitigate offset voltage, skew, and jitters, a digital comparator and clock network must be designed. Similarly, raising the clock signal slew rate reduces the switching duration, reducing the amount of time that noise is present during the threshold period. As a result, the comparator has also demanded a portion of the Flash ADC. The proposed CITIQ comparator, which is built digitally with the aid of a clock circuit to reduce jitter and increase the slew rate (Slew Rate=$2fV_{pp}$) to minimize skew, sort out the above factors. This CITIQ comparator compares the analogue electrical potential to the reference voltage to propagate the thermometer code, and then an adaptive bubble free logic circuit identifies and corrects any bubble faults that might occur in that thermometer code. Finally, the binary encoder outputs binary codes from the bubble free code.

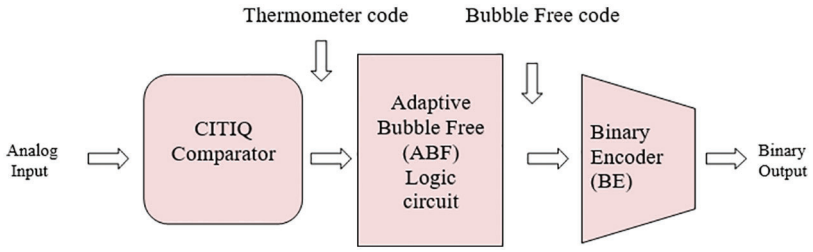

Figure 1: Blocks involved in C-Flash ADC

3.1 Proposed CITIQ Comparator

A group of resistors from the ladder circuit is used to produce a comparator reference voltage in a typical flash ADC. The comparator must be large because the reference potential produced by the group of resistors in the circuit consumes more power. It can be overcome by CITIQ comparator technique. This paper proposes a CITIQ comparator with a small size and low power consumption. A CITIQ comparator, made up of two CMOS inverters and a dual set of NMOS and PMOS transistors, compares the analogue input potential to an internally generated reference potential and provide a binary output. Internal reference voltages are produced from the threshold voltage (V_t), eliminating the need for a resistor ladder circuit in the Flash ADC. The CITIQ comparator compares the input voltage to the internally created reference potential, which is resolved by changing the width of the transistors, which is the first stage of the cascading structure. Obtain sharper threshold and full output voltage swing by using the succeeding stage of the cascading structure called a gain booster.

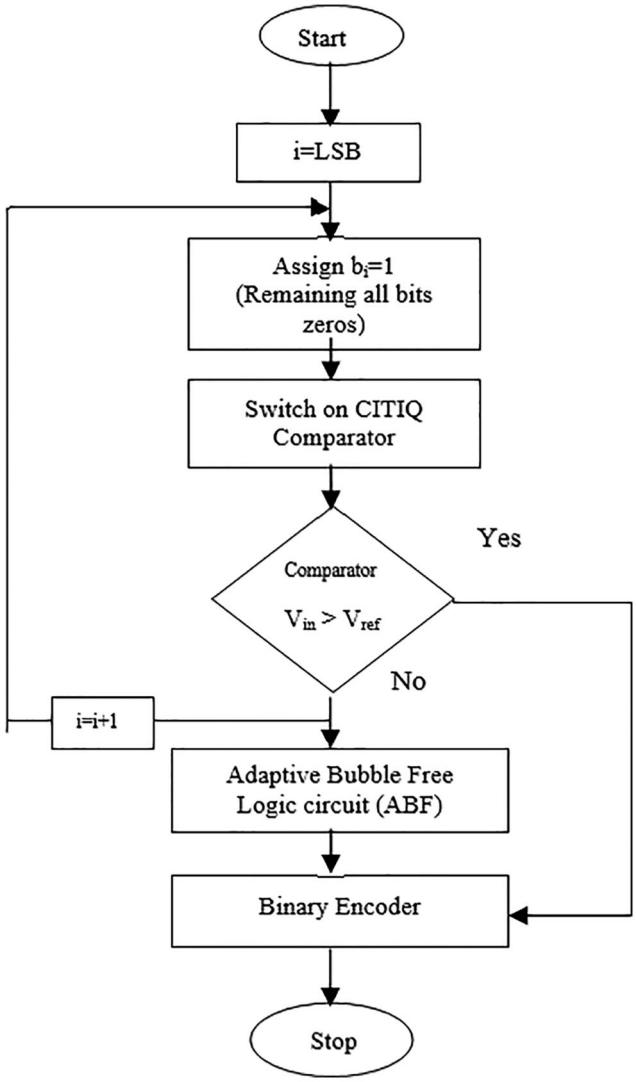

Figure 2: Flow chart of proposed C-FADC

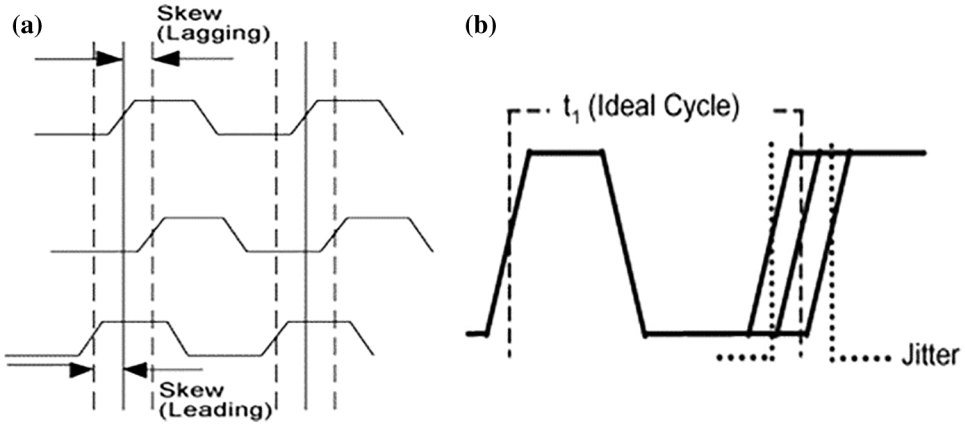

Figure 3: (a) Clock skews (b) Jitter

The schematic view of the proposed single stage Clocked ITIQ comparator is shown in Fig. 4. It employs a pair of cascaded inverters with PMOS 1, PMOS 2, and the NMOS 1 as the ITIQ comparator, as well as two sets of the PMOS 4, NMOS 2, and PMOS 5, NMOS 3 transistors connected in parallel. The ITIQ comparator networks are pulled down and up by each pair. A clock pulse guides the pair of PMOS and NMOS transistors; the NMOS is linked to the clock, while the PMOS is linked to the clock bar. Internally, the CITIQ comparator generates a reference voltage; the length (L) and width (W) of PMOS and NMOS are varied to obtain the desired switching voltage. The comparator switching voltage is determined by the NMOS and PMOS threshold voltages. To reduce the design power consumption, the threshold voltage should not be deviated too far. In contrast, regardless of whether the transistor length is held very short to achieve a speed, channel noise can affect the output, resulting in a nonlinear switching pattern. As a result, the transistor length (L) is set at a nominal value, and the width of the transistor is used to generate different switching voltages. As the transistor width (W) is increased, the transistor current drive capability increases, reducing the signal rise or fall time at the gate terminal's output. The active area of active devices increases with increased transistor size and the layout area may increase.

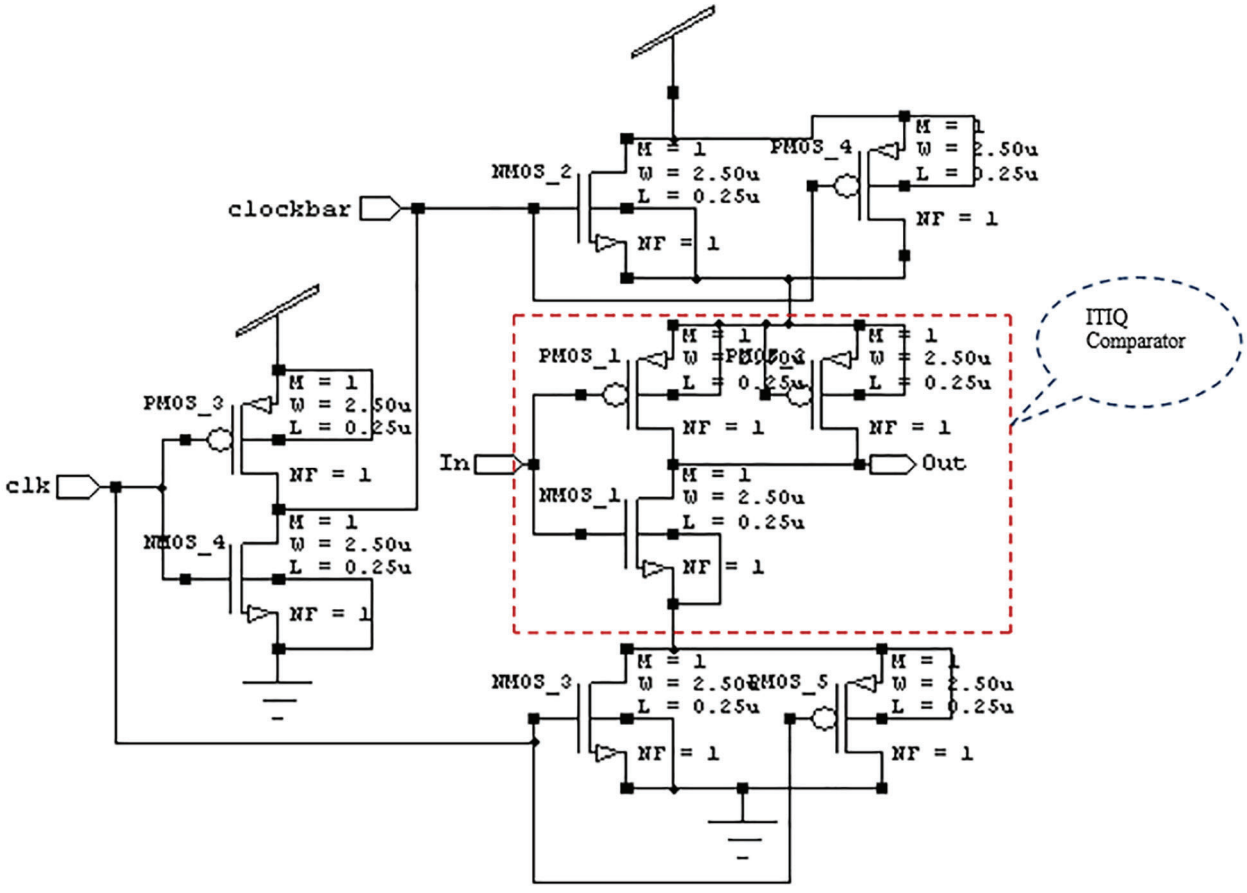

Figure 4: Schematic view of clocked ITIQ comparator

The mathematical Eqs. (1)–(4) used to choose these switching potentials are as follows:

$$V_s = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_p}} \cdot V_{AIR}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_p}}} \tag{1}$$

Analog Input Range (AIR) voltage

$$V_{AIR} = [(V_{dd} - |V_{tp}|) + V_{tn}] \tag{2}$$

Minimum size variation of transistor

$$V_s = \frac{V_{dd}}{2} \tag{3}$$

The least significant bit (LSB for n-bit) voltage

$$LSB = \frac{V_{AIR}}{2^n - 1} \tag{4}$$

where,

W_p is the PMOS transistor width

W_n is the NMOS transistor width

V_{dd} is the source potential

V_{tn} is the NMOS transistor threshold voltage

V_{tp} is the PMOS transistor threshold voltage

μ_n is the mobility of electron

μ_p is the mobility of hole

It is expected that the NMOS length (Ln) = PMOS length (Lp). The transistor parameters of CITIQ comparator are shown in Tab. 1. The switching voltage was determined by initially varying NMOS transistor sizes, (1.25–2.8 μm) and then maintaining a constant value (3 μm). Tab. 2 also shows the different sizes of PMOS transistors (0.21–3.72 m). Based on the comparator switching voltage, the LSB (Least Significant Bit) for n-bit is 0.106 V.

Table 1: Transistor parameters of CITIQ comparator

Parameter	Value
$W_p$max	3.72 μm
$W_n$max	3.00 μm
$W_p$mim	0.21 μm
$W_n$mim	1.25 μm
$L_n = L_p$	0.25 μm
μ_p	240 cm^2/Vs
μ_n	340 cm^2/Vs

Table 2: Switching voltage for CITIQ comparator design

Width of NMOS (W_n) µm	Width of PMOS (W_p) µm	Switching Voltage(V_s)
1.25	3.72	0.95
1.74	3.63	0.87
2.5	3.43	0.79
2.8	3.11	0.77
3	3.02	0.73
3	2.84	0.71
3	2.53	0.69
3	2.34	0.68
3	2.11	0.65
3	1.77	0.62
3	1.48	0.59
3	1.25	0.56
3	0.97	0.51
3	0.68	0.45
3	0.44	0.38
3	0.21	0.29

3.2 Adaptive Bubble Free (ABF) Logic Circuit and Binary Encoder (BE)

The binary or parallel encoder is used to convert a 15-bit comparator output to a 4-bit digital word, with Adaptive Bubble Free (ABF) logic to eliminate bubble faults from the thermometer code. One or more bits of invalid code which be created by a bubble fault in the thermometer code. It is classified by the quantity of invalid 0 Bit between 1 Bits named as 1st order, 2nd order, 3rd order and 4th order bubble faults. The bubble-free circuitry has fifteen 3-input NAND logic gates and fifteen inverters and is inserted between the comparator and binary encoder. Eight 4-input NAND logic gates and four 2-input OR logic gates make up the binary encoder circuit. Fig. 5, shows the functional blocks of the Adaptive Bubble Free logic with Binary Encoder. The following Eqs. (5)–(8) illustrate the Boolean expression that relates the predicted binary output E_3 –E_0 obtained from the binary encoder using adaptive bubble free logic circuit.

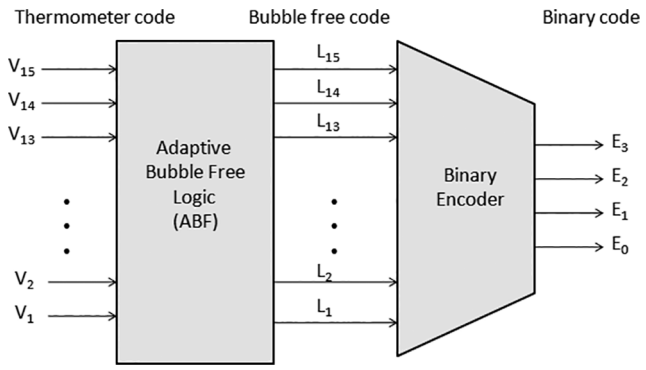

Figure 5: Functional blocks of an adaptive bubble free logic with binary encoder

$$E_0 = \overline{L_1 L_3 L_5 L_7} + \overline{L_9 L_{11} L_{13} L_{15}} \quad (5)$$

$$E_1 = \overline{L_2 L_3 L_6 L_7} + \overline{L_{10} L_{11} L_{14} L_{15}} \quad (6)$$

$$E_2 = \overline{L_4 L_5 L_6 L_7} + \overline{L_{12} L_{13} L_{14} L_{15}} \quad (7)$$

$$E_3 = \overline{L_8 L_9 L_{10} L_{11}} + \overline{L_{12} L_{13} L_{14} L_{15}} \quad (8)$$

The bubble fault examples in the thermometer code are shown in Tab. 3. There are four types of bubble faults mentioned in that table are 1st order, 2nd order, 3rd order and 4th order. If the 1st order fault identified, in a regular situation, the correct sequence may be 000000000000011 or 000000000001111. Getting 1st order fault in the table, in normal condition, the correct sequence is 000000000000011 or 000000000001111. Nonetheless, the bubble fault happens in the bit V_3 for this situation, so it makes the succession frail as 000000000001011. A comparative circumstance occurs with 2nd order, 3rd order and 4th order bubble faults. These bubble faults are corrected by an adaptive bubble fault free circuit.

Table 3: Bubble faults – Example

Fault type	Thermometer code with bubble faults (V_{15} to V_1)
1st order fault	000000000001**0**11
2nd order fault	000000000001**00**11
3rd order fault	0000001**000**11111
4th order fault	001**0000**11111111

Tab. 4 shows the truth table of the Adaptive Bubble Free logic and binary encoder. From this table it is observed that the subsequent code of the CITIQ comparator arrangement named thermometer code with bubble faults is noted by V_{15} to V_1, the outputs of the adaptive bubble free logic circuit is represented by L_{15} to L_1 and the encoded binary output indicated by E_3 - E_0. The combination of adaptive bubble free logic circuit and binary encoder is linked to accomplish fast over the current encoders, for example, Fat tree structured encoder, ROM encoder, and Multiplexer based encoder and Priority encoder.

4 Results and Discussion

S-Edit (Tanner EDA Tool) is used to implement the 4-bit C-FADC schematic in 0.25 μm CMOS Technology, and T-Spice is used to simulate it. The W-Edit displays the output waveforms.

4.1 Simulation Result of CITIQ Comparator

Fig. 6, shows the simulation outcome of a single stage CITIQ Comparator. In Tab. 5, the power utilization and propagation delay for different comparators are evaluated. As compared to Open Loop Comparator, Quantum Voltage Comparator, Threshold Inverter Quantization Comparator, and Improved Threshold Inverter Quantization Comparator, the recommended CITIQ comparator plan reduces the utilization of power by 81.54% 76.52%, 72.72%, and 58.0% respectively. The power utilization and propagation delay evaluation for various comparators is depicted in Fig. 7. From this chart, it is seen that the proposed Clocked ITIQ comparator design decreases the propagation delay by 40.45%, 29.09%, 21.21%, and 17.74% when compared to Open Loop Comparator, Quantum Voltage Comparator, Threshold Inverter Quantization Comparator, and Improved Threshold Inverter Quantization Comparator respectively. Eq. (9) is used to measure the propagation delay, which is given as,

Table 4: Truth table of an adaptive bubble free logic and binary encoder

Thermometer code with Bubble faults (V_{15} to V_1)	Adaptive Bubble free logic output (ABF) (L_{15} to L_1)	Encoder output (E_3 to E_0)
000000000000000	1111111 11111111	0000
000000000000001	111111111111110	0001
000000000000011	111111111111101	0010
000000000000111	111111111111011	0011
000000000001**0**11	111111111110111	0100
000000000001**00**11	111111111101111	0101
000000000111111	111111111011111	0110
000000001111111	111111110111111	0111
000000011111111	111111101111111	1000
000000**000**11111	111111011111111	1001
000001111111111	111110111111111	1010
000011111111111	111101111111111	1011
000111111111111	111011111111111	1100
001**0000**11111111	110111111111111	1101
011111111111111	101111111111111	1110
111111111111111	011111111111111	1111

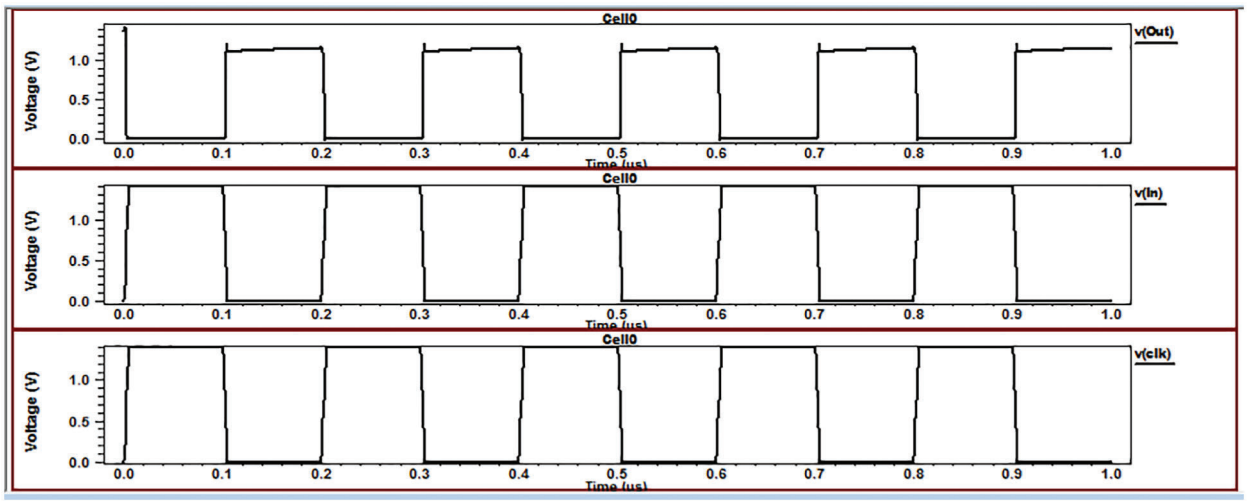

Figure 6: Simulation result of CITIQ comparator

$$t_p = \frac{\left(t_{plh} + t_{phl}\right)}{2} \tag{9}$$

where,

t_{plh}- Rising propagation period.

t_{phl}- Falling propagation period

Table 5: Power utilization and propagation retard for various comparator

Comparator array	Power utilized (mW)	Propagation delay (µSec)
Open Loop Comparator (OLC)	5.783	2.62
Quantum Voltage Comparator (QVC)	4.545	2.20
Threshold Inverter Quantization (TIQ) Comparator	3.912	1.98
Improved Threshold Inverter Quantization (ITIQ) Comparator	2.541	1.86
Clocked Improved Threshold Inverter Quantization (CITIQ) comparator (proposed)	**1.067**	**1.53**

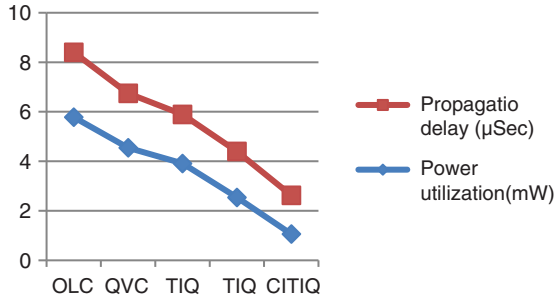

Figure 7: Power utilization and propagation retard evaluation of various comparators

4.2 Simulation Result of Binary Encoder and Adaptive Bubble Free Logic Circuit

The power utilization and transistor count comparison of different encoding plans is presented in the Tab. 6. As compared to FTE (Fat Tree Encoder) with Bubble Free circuit, ROME (ROM Encoder) with Bubble Free circuit, MUX-E (Multiplexer based Encoder) with Bubble Free circuit and PE (Priority Encoder) with Bubble Free circuit, the suggested Binary encoder reduces the utilization of power by 76.49%, 74.59%, 65.81%, and 62.8%, and also minimizes area by 44.91%, 44.62%, 42.13% and 36.02%.

Table 6: Power utilization and transistor count comparison of different encoding plans

Encoder types	Power utilized (mW)	Transistor count
Fat Tree Encoder(FTE) +BFC	9.254	374
ROM Encoder(ROME) +BFC	8.562	372
MUX-Encoder (MUX-E) +BFC	6.362	356
Priority Encoder (PE)+ BFC	5.860	322
Binary Encoder (BE)+ ABFC (Proposed)	**2.175**	**206**

4.3 Graphical Response and Outcomes of C-FADC

Fig. 8, shows the graphical response of the Clocked FADC. The 4 Bit Clocked FADC is designed and implemented using Tanner EDA Tool and 250 nm CMOS technology. In terms of area, power utilization, speed, and resolution quality, the Flash ADC performance is examined. The comparison of Power

utilization, Reliability and Throughput for different FADCs is listed in Tab. 7. As compared to OLC –FTE ADC, QVC –ROME ADC, TIQ –MUXE ADC, and ITIQ – PE ADC, the desired Clocked FADC brings down the power utilization by 78.45%, 75.28%, 68.45%, and 61.42% less.

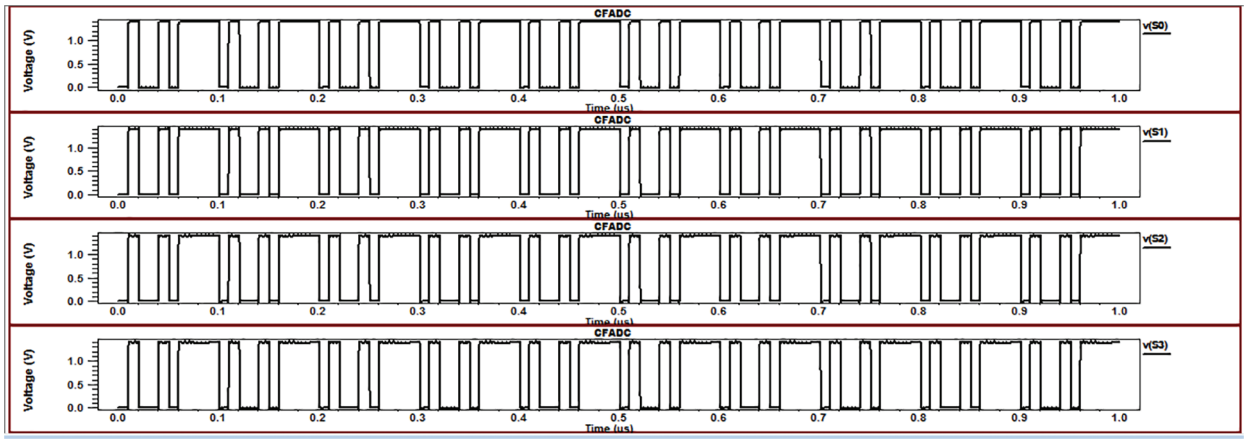

Figure 8: Graphical response of clocked FADC

Table 7: Comparative analysis of C-FADC with various ADCs

FADC Techniques	Power Utilization (mW)	Reliability (%)	Throughput Rate (ns)
OLC –FTE ADC	15.04	75	56.2
QVC –ROME ADC	13.11	83	47.1
TIQ –MUXE ADC	10.27	88	32.4
ITIQ- PE ADC	8.40	95	20.5
CITIQ-BE ADC (C- FADC)	**3.24**	**97**	**9.09**

When compared to the ITIQ-PE ADC, the proposed CITIQ-BE ADC (C-FADC) achieves a throughput rate of 55.65% and a reliability of 97%. In comparison to the evaluation results, the proposed Clocked FADC outperforms the multiple organized FADCs. Fig. 9, shows the throughput comparisons for various FADC techniques. The DNL and INL results are obtained at 500 MHz Virtual Resolution Bandwidth (VRB), and the deliberate SFDR (Spurious Free Dynamic Range) is 29.3 dB for the input frequency 85 MHz, as noted by the 10th harmonic. The FFT spectrum performance of the C-Flash ADC is shown in Fig. 10 and the SNDR (Signal to Noise Defined Ratio) obtained from that spectrum is 23.2 dB.

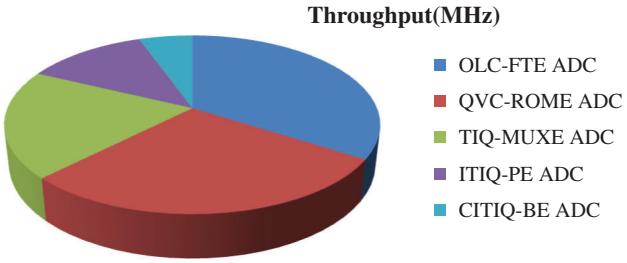

Figure 9: Comparison of throughput for different FADC techniques

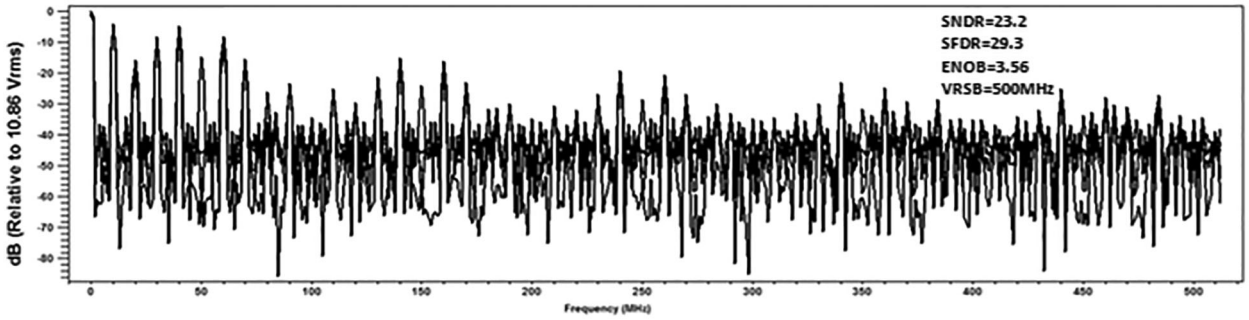

Figure 10: FFT spectrum output of C-Flash ADC for VRB 500 MHz

The peak differential nonlinearity is +0.65/−0.65 LSB, and the integral nonlinearity is +0.45/−0.5 LSB, as shown in Fig. 11. (i to iv). The proposed FADC utilizes the power is 3.24 mW for a supply potential of 1.4 V and achieves 3.56 effective numbers of bits at 1.2 GS/s. The figure of merit (FOM) is defined as FOM = Power/ (2.VRB.2^{ENOB}). As such, the calculated figure of merit is 0.274 pJ/conv.-step and the summary of static and dynamic parameters of the C-FADC observed from the FFT spectrum is noted down in Tab. 8. The balance between power, speed of execution, and circuit efficiency is clearly surveyed using the Force Delay Product (FDP) thing. When conversion latency is taken into account, the C-FADC arrives at 0.14 pJ - ns/conv. - step, according to the deliberate FDP item.

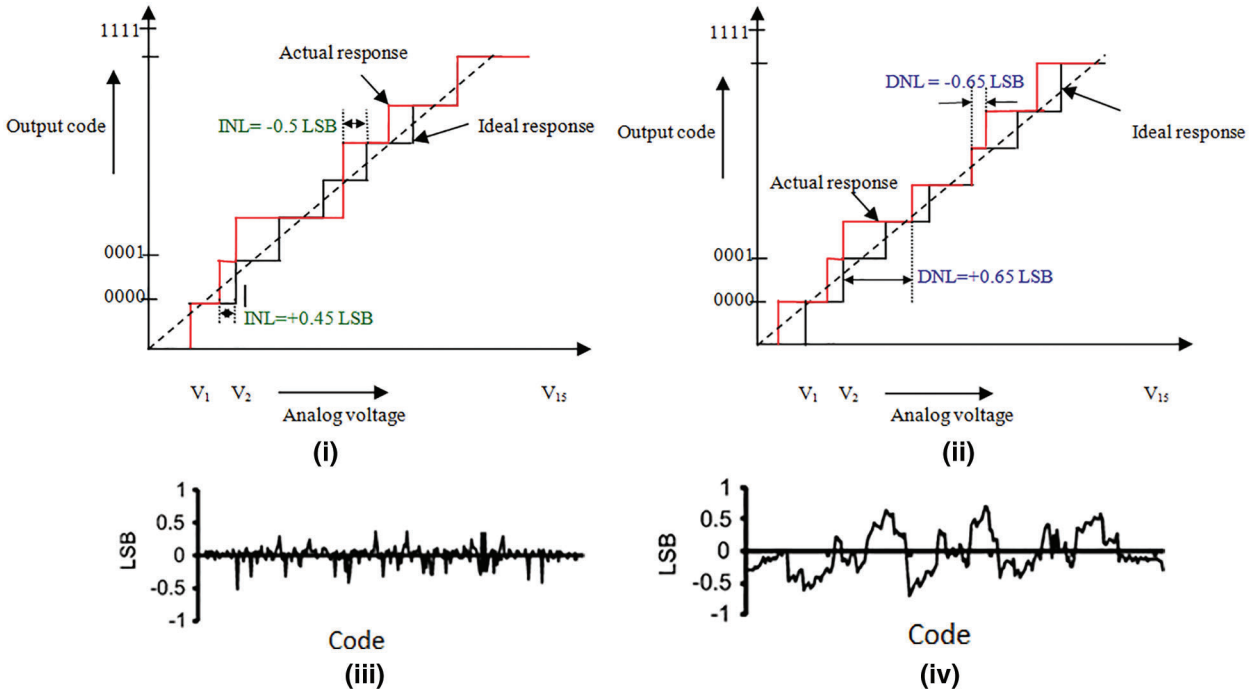

Figure 11: (i) and (iii) Integral Non-linearity, (ii) and (iv) Differential Non-Linearity at 500 MHz Virtual resolution bandwidth

The C-FADC results and reference to the state-of-the-art are shown in Tab. 9. It is demonstrated that in FADC architectures, the arranged Clocked Flash ADC can achieve incredible one-of-a-kind execution and a superior balance between Speed, Power, FOM, and VRB. In comparison to the references [1,2,4,7,8,10,11,14,15,19,20,22], the exhibited work uses low power 3.24 mW, and the Figure of Merit (FOM) is lower than the authors [4,8,10,14].

Table 8: Summary of static and dynamic parameters: C-FADC

Parameter	Results (Proposed method)
Architecture	C-FADC
Technology	250 nm
Resolution	4 bit
Supply Voltage	1.4 V
Speed	1.2 GS/s
Switching Voltage Range	0.29V<Vs<0.95
Power Utilized	3.24 mW
Reliability	97%
SNDR	23.2 dB
SFDR	29.3 dB
FOM	0.274pJ/con.-step
DNL	+0.65/−0.65 LSB
INL	+0.45/−0.5 LSB
Conversion time	13.2 nsec
FDP	0.14 pJ-ns/conv.-step
Slew Rate	0.75 V/μs

Table 9: C-FADC results and comparison with state-of-art

	Speed (GS/s)	Supply (v)	Power (mW)	Resolution (bits)	Process (nm)	ENOB	SNDR (dB)	SFDR (dB)	DNL (±LSB)	INL (±LSB)	FOM (pJ/Conv-step)
Proposed Work	**1.2**	**1.4**	**3.24**	**4**	**250**	**3.56**	**23.2**	**29.3**	**+0.65/ –0.65**	**+0.45/ –0.5**	**0.274**
[1]	1	1.2	10.5	6	130	5.26	33.42	45.71	–0.41/ +0.50 ±0.3	–0.77/ +0.52 ±0.35	0.02
[2]	1	0.7	3.57	6	28	5.88	37.15	39			0.06
[4]	0.4	1.8	18.62	5	180	4.78	30.56	42.04	0.206	0.218	1.69
[7]	1.6	2.25	12	6	180	5.7	–	–	+0.4/ –0.4	+0.4/ –0.4	–
[8]	1.5	1.2	23	4	90	3.69	–	–	–	–	1.18
[10]	3.2	1.2	120	5	130	4.54	–	–	+0.18/ –0.24	+0.39/ –0.29	4.30
[11]	1	1	15.75	6	90	5.76	36.45	45	0.08	0.1	0.29
[14]	1.2	1.5	160	6	90	–	35.8	46	0.4	0.6	2.2
[15]	2	1.8	35	6	180	5.06	32.25	–	–	–	0.27
[18]	1.25	1	0.595	5	65	4.37	28.07	36.56	0.67	0.47	0.023
[19]	0.2	1.8	4.51	4	180	3.7	24.4	30.2	±0.25	+0.6	–
[20]	1.5	1.2	204	7	90	6.05	38.17	46.6	0.7	0.64	–
[22]	5	1	7.8	5	65	–	26.19	34.22	0.83	0.79	0.094

5 Conclusion

Tanner EDA is used to build and simulate a 4-bit low-power and high-speed Clocked Flash ADC (C-FADC) that works with 1.4 V input source voltage. From the clocked ITIQ comparator, the clock

network diminishes the jitter by minimizing the propagation delay with the switching voltage range is 0.29 V<Vs<0.95 V and achieves the high slew rate is 0.75 V/μs to reduce skew. The adaptive bubble-free logic circuit corrects bubble faults up to fourth order, while the binary encoder transforms the bubble-free code into binary code. With a Virtual Resolution Bandwidth (VRB) of 500 MHz and a speed of 1.2 GS/s, this newly built architecture achieves a FOM of 0.274 pJ/conv.step. The signal to noise distortion ratio is 23.2 dB and spurious free dynamic range is 29.3 dB observed from the FFT-spectrum at 85 MHz input frequency. By using this proposed structure, it is possible to achieve the effective number of bits is 3.56 and the force delay product is 0.14 pJ-ns/conv.-steps. The designed C-FADC structure achieves 97% reliability and has the differential and integral non linearity is ±0.65 LSB and +0.45/−0.5 LSB respectively.

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