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Field Programmable Gate Arrays (FPGA) Based Computational Complexity Analysis of Multicarrier Waveforms

C. Ajitha[1,*] and T. Jaya[2]

[1]Department of ECE, University College of Engineering, Nagercoil, Tamilnadu, 629004, India
[2]Department of ECE, CSI Institute of Technology, Thovalai, Tamilnadu, 629302, India
*Corresponding Author: C. Ajitha. Email: ajitha14ucen@gmail.com
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Abstract: Multicarrier waveforms with enhanced spectral efficiency, low latency, and high throughput are required for 5G wireless networks. The Orthogonal Frequency Division Multiplexing (OFDM) method is well-known in research, but due to its limited spectral efficiency, various alternative waveforms are being considered for 5G systems. In the recent communication world, NOMA (non-orthogonal multiple access) plays a significant part due to its wider transmission of data with less bandwidth allocation. Even if a high data rate can be attained, the transmission problem will arise due to the spread of multiple paths. In order to reduce complexity and area utilization, a novel PL-based FWFT (Fast walsh hadamard fourier transform) technique is proposed and implemented in the VLSI architecture. To achieve a high-performance system, the main concept of pass transistor logic (PL) with VLSI implementation is to diminish the size and power consumption. Finally, the performance of the proposed FWFT/ IFWFT implementation has been evaluated. For FPGA's 16-point FWFT, the number of transistors decreased by 21% and the total power required was reduced by 5.5%. The same implementation for 34 transistor-pass-logic customs and power consumption is 2.764 mW with a latency of 78.256 ns. As a consequence, the proposed system achieves low power, area and low complexity system that can enhance the function of the multicarrier waveform systems.

Keywords: Fast walsh hadamard fourier transform; FPGA; pass logic transistor; multiple input multiple outputs

1 Introduction

Wireless communication Beyond 5G (B5G) network goal is to enable many changes in the network related to quality and volume of the services such as low latency network communication [1], massive data transfer, augmented reality requires a more convenient network to perform this with more reliability. The Orthogonal Frequency Division Multiplexing (OFDM) method is well-known in research, but due to its limited spectral efficiency, various alternative waveforms which includes Filter Bank Multicarrier (FBMC) [2], Generalized Frequency Division Multiplexing (GFDM), Universal-Filtered Multicarrier (UFMC) and RB-adaptive F-OFDM [3]. To improve the spectral efficiency, Cyclic Prefix is inserted to

the OFDM as (CP-OFDM), but FBMC can perform the transmission without CP. But the inter symbol interference makes the transmission signal to be attenuated, making it unsuitable for low latency states [4]. Although UFMC is considered for low latency scenarios, it's out of band emission limited the transmission efficiency. The above multicarrier waveforms are elaborately listed below,

1.1 CP-OFDM

The notable CP-OFDM multicarrier waveform will be utilized without a doubt in future 5G advancements, since it gives great execution while keeping simplicity. The rule of OFDM is to separate the entire data transmission, so that channel adjustment can be regularly decreased [5]. In CP OFDM, the latter part of the OFDM frame's data is added to the beginning of the OFDM frames to prevent inter-symbol interference (ISI) or inter-band interference in OFDM, and the length of the cyclic prefix should be higher than the channel delay spread. Furthermore, the channel delay spread varies with frequency, and the CP length should be broad enough to accommodate for both interferences and can be adaptable [6].

1.2 RB-F-OFDM

The transmission or else receipt part utilized in entire RBs is the identical, so it receipts advantage of existence modular and scalable. PTS and SLM are two roles included in the RB-F-OFDM framework [7] that help to reduce PAPR. The process of removing RB-F-OFDM enabled PAPR and increasing the efficiency of the provided device is known as phase rotation. Rayleigh's distribution channel can be used to achieve a higher SNR value, resulting in improved system performance. The polyphase implementation of the IoT RB-F-OFDM system proposes a new transformation to minimize the PAPR and complexity. The system complexity in OFDM, FFT [8] is used because of IFFT at the transmitter and receiver, but this is condensed by FWFT and therefore decreases PAPR.

1.3 FBMC

Channel bank-based waveforms don't need cyclic prefix and accomplish great spectrum regulation and better side projection constrictions offering essentially improved capacities when managing the obstruction created by offbeat transmissions. In any case, the usage unpredictability of channel banks is higher than that of CP-OFDM frameworks [9]. FBMC subcarriers are ideally planned in the recurrence space to give spectrum conservativeness, these waveforms needn't bother with a CP and accordingly are more spectrum effective. FBMC-QAM and FBMC-OQAM are the two option multicarrier waveforms dependent on the FBMC idea.

1.4 GFDM

Generalized Frequency Division Multiplexing (GFDM) [10] is widespread with another idea and is made out of non-orthogonal subcarrier which spread the information as time and recurrence domain. In order to evade inter-symbol interference, a CP is added toward the termination of each square of images and gives a low latency signal on account of circular separating with model channels [11]. To improve the spectrum productivity, the tail biting method can be applied to diminish the CP length. To additionally progress the spectrum area, a windowing cycle can be included in the transmitter.

1.5 UFMC

The UFMC waveform [12] is a subset of the OFDM waveform combined with post-separating, in which a group of transporters is sorted by utilizing a recurrence area proficient usage. Scientists are currently working on various plans [13] and experimenting with new waveforms [14]. UFMC conspire, that can overcome the constraints of OFDM, the speculation of OFDM and FBMC system is UFMC. It upholds low latency and quick time division duplex exchanging.

Due to its configurable circular shaping filters, NOMA [15] has taken abundant consideration in later scenery, versatility features such as small level OoB discharge, and its adaptability related to non-OFDM based waveforms [16]. NOMA can utilize non-contiguous spectrum chunks to transmit the signal through carrier aggregation techniques; but this is not possible for OFDM technique. In additional, NOMA is more spectral efficient and each block needed one CP and each block consists of many subcarriers and subblocks. Prototype filters are used to attract more NOMA features, requiring more hardware execution than OFDM. In order to ease the difficulty, low-complexity modulation/demodulation plans are quickly presented.

Another interesting technology for improving spectrum efficiency is cognitive radio (CR) [17]. The secondary user (SU) has access to the spectral range that is allocated to the primary user in CR (PU). As a result, cognitive NOMA anticipates more efficient spectrum allocation. The pairing of NOMA and CR is thought to be capable of enhancing spectrum efficiency even more (SE). Spectrum sharing has been extensively used because of its minimal complexity. It has been demonstrated that employing NOMA in CR improves SE substantially when contrasted to using OMA in CR. The functional differences of NOMA from OMA, the spectrum cannot be simultaneously accessed by users. In NOMA, multiple users can simultaneously access the available spectrum [18]. Therefore, NOMA is recognized as a strong campaigner among all other technologies because it has the important accent of overcoming the difficulties in OMA.

The complexity of the MIMO technique is another great real time problem. Thus, the complexity of this paper is concerned and reduced by the use of the FWFT algorithm. Instead of using FFT, here FWFT [19] is used because FWFT needs only fewer stages of multiplication compared with FFT which reduces the complexity and power consumption.

- FFT: For N subcarriers number of stages = N/2 $\log_2$ (N).
- FWFT: For N subcarriers number of stages = $\log_2$ (N)-1.

Basically, an IFWFT is a transform technique which is the pair of IDFT and IWHT. When compared IFFT, IFWFT has less complexity [20] and less resources. Ce Kang et al proposed an OFDM system with FWFT and PEC method to decrease the complexity range by using Piece-wise exponential companding, and the transform value is calculated based on fast wash- Hadamard function. Jinqi Liu et al proposed a pipeline structure for FWFT. In recent years FWFT is an important term to find the transform parameters. The planned architecture decreases the quantity of buffers by 50 percent and adders by 25 percent. But FWFT's real time is not a satisfactory function, so FWFT is implemented in the VLSI structure to convert the system into a fixed real-time application. The achievement of high-performance multicarrier generation system, pass transistor logic (PL) based VLSI implementation is used to decrease the size and power consumption.

The rest of the paper is systematized as follows: Detailed literature of the FPGA-based NOMA system is described in Section 2. The proposed methodology of the novel FWFT method for the transmission of NOMA and the Pass Logic Circuit is described in Section 3. The implementation of hardware and FPGA can be discussed in Section 4. Experimental outcomes and complexity results have been simulated in Section 5. Finally, the conclusion arrived is presented in Section 6.

2 Related Works

Chin-Teng Lin et al proposed a pipeline radix-4^2 which adopts a multiplexer with a CFA to support a 256-point FFT. To reduce multiplier cost and Size, Segment Shift Register and Overturn Shift Register is used. The outcome of FPGA Chip uses 22.37 mW at 100 MHz in TSMC. Bo-Ting Wang et al proposed a low-voltage SOI CMOS Complementary (CPL) circuit to control figure partiality of pass transistor

through one of secondary transistor. Even though this method is good, it only gives the best result in serially-connected multiple inputs. Ramya Devi. K et al proposed Vedic mathematical techniques to reduce the complexity in the FFT technique. Vedic mathematics contains 16 sutras which are mathematical shorthands for a range of operation covering basic arithmetic's, algebraic. Marrio Garrido et al proposed an FFT based radix-4 memory system. This Construction requires entire memory size N and also some extra multiplexers. The NOMA scheme is implemented in real-time using a field-programmable gate array (FPGA), which is an appealing and effective approach. This is because FPGAs provide designers more flexibility in terms of modifying developed systems while maintaining the maximum possible throughput. Finally, there is a less amount of distributed logic using FPGA implementation with referred to DSP slices was obtained. Real-time FPGAs are used to build MIMO systems with OFDM in which an iteration receiver is recommended, in order to minimize delay and complication. Ricardo Gonzalez-Toral et al proposed a Concurrent error detection technique that is used such as DMR, FFT, these techniques are implemented on SRAM based FPGAs. When detecting the errors of complex FFT using the SoS technique, the outcome is better.

Kazuo Yano et al proposed a CPL to the whole dangerous track. The CPL comprises of CMOS, an NMOS pass-transistor rationale organize, and complementary inputs/outputs earns inverters. Basically, multiplication time is fastest method compared with other methods. Anbarasan et al explained OFDM applications using FFT processing and VLSI implementation and IFFT processors also reduce the power and chip area with the help of processing elements. Teng Su et al recommended the combined form about WHT and DFT into an on the single algorithm which is called as fast Hadamard–Fourier transforms algorithms. The algorithm produces the scant matrices for each step-in radix-R mode.

2.1 Existing Fast Fourier Transform Techniques

The reason why FWFT is used instead of FFT is, it uses only a few multiplication and addition stages. For instance, to compute a 16-point FFT, radix-4 proceeds only $log_4 16 = 2$ stages. Being the radix-4 FWFT needs lesser stages and BF compared radix 4 FFT, calculation of FWFT can be extra upgraded. To compute a 16 point, the radix-4 receipts only $(log_4 16)-1 = 1$. But for FFT, it needs two stages, but in FWFT, it only needs only one stage. So, the complexity range will also decrease. In FFT multiplication complexity is reduced based on the twiddle factor. The input of N-point grouping x(n) into quadruple sub-orders x(4n), x (4n + 1), x (4n + 2) and x (4n + 3) are part of a radix-4 FFT measurement. By choosing L = 4 and M = N/4 within a bound together process, the radix-4 FFT calculation remains accomplished. This corresponds to n = 4m + 1 and k = (N = 4) p + q. The calculations of radix-4 FFT are got via taking after the decomposition strategy laid out within the past segment v times recursively. In FFT, the fast algorithm is used to calculate the Fourier transform values and for FWFT, another one fast algorithm is used to calculate WHT and DFT simultaneously Monir T. Hamood et al proposed a (FFT-WHT), which determines the fast Fourier transform and Walsh–Hadamard transform. It reduces the implementation cost and complexity and keeps about 70%–36% in computer duration towards n transforms lengths of 16–4096.

2.2 Complexity Comparison

- Number of stages required for complex multiplications (FFT) $= \dfrac{N}{2} log_2 N$
- Number of stages required for complex additions (FFT) $= N log_2 N$
- Number of complex multiplications (FWFT) $= \dfrac{1}{2} [N log_2(N) - (2N - 2)]$
- Number of complex additions (FWFT) $= \dfrac{3}{2} [N log_2(N) - (2N - 2)]$

In Fig. 1, 16-point radix 4 FFT has 32 complex multiplications and 64 complex additional stages. But the 16-point radix 4 FWFT uses 17 multiplication and 51 additional stages. As a result, the number of stages required for FWFT is very low compared to the number of stages used in FFT. Thus, the complexity range is reduced and implemented in VLSI to make this system a real-time application.
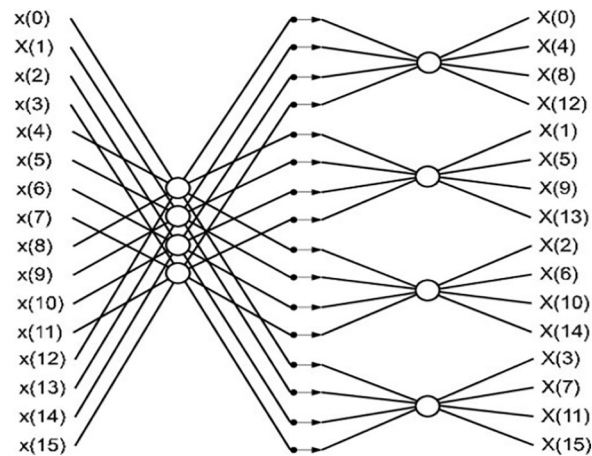

Figure 1: Radix-4 16-point FFT BF structure

Fig. 2 shows the structure of the FWFT BF for 16-point radix-4. There is a low amount of real-time addition in radix-4 FWFT and multiplication is required. Four points are added to each stage and the values are calculated to be sent to the next stage of the BF. In addition, one more expansion may be reduced by the use of the butterfly structure and 3 multiplication and 15 additions are used for each butterfly.
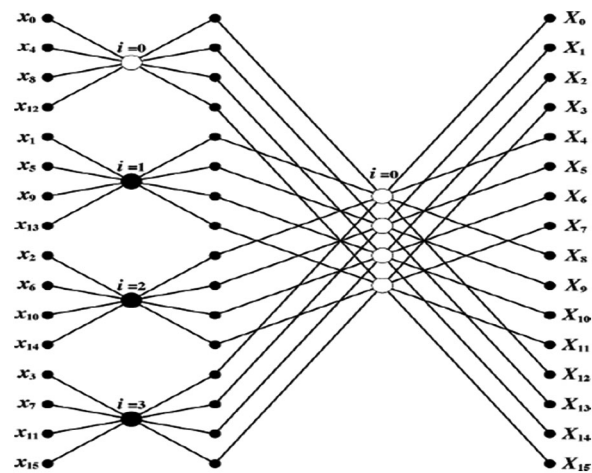

Figure 2: FWFT 16-point radix-4 BF structure

3 Proposed Methodology

In the proposed method, a novel FWFT algorithm is used to achieve a very low complexity of the NOMA system and most importantly, the time requirement for the proposed methodology is very low with the help of the logic circuit. After determining the FWFT value, this system is implemented in the VLSI architecture to make the NOMA system a real-time purpose.

Block diagram of pass logic circuit based FWFT shown in Fig. 3, it consists of a small amount of addition and multiplication in real time. The adder for real-numbers is compatible with the subtractor. Real and imaginary components interweave the input/output data. In FWFT there are many multipliers are presented at the input side to multiply real and imaginary part of the butterfly values. The multipliers in the input stage Radix-4 butterflies accept one input, m as somewhat of {–1, 0, +1}. Those values are replaced into PL which takes m as any one of {11,00,01,10}. Here the pass logic played an important role because it replaced the multipliers with a single circuit so, the transistor required for those methods will better. The area and power need for this technique are very low. Pass logic frequently customs less transistors, scores faster, and wants less power than CMOS logic. The first stage data processing order for the 16-point FWFT system for NOMA transmission is discussed below,
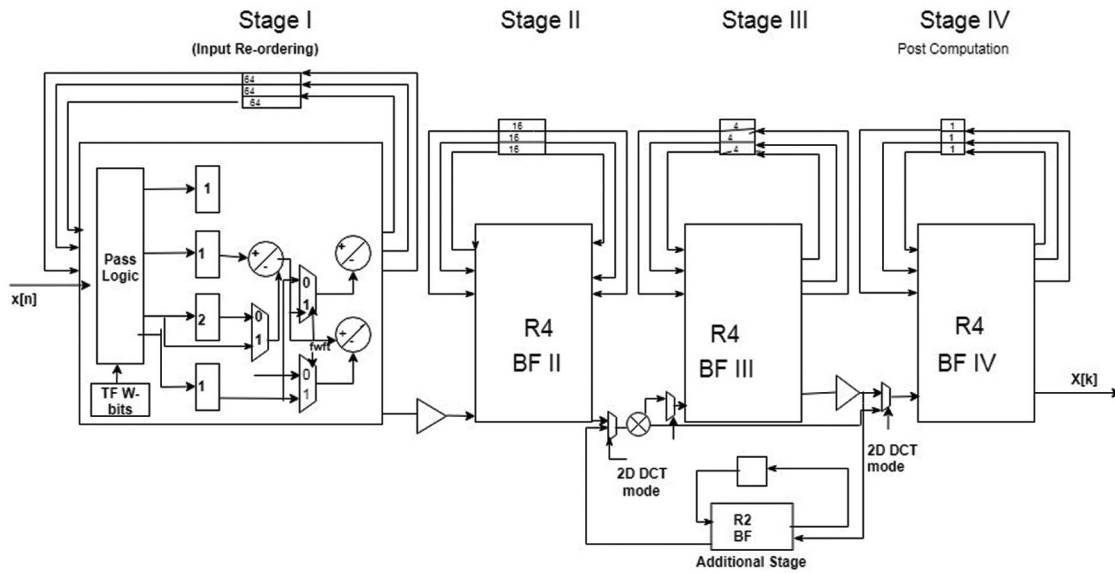

Figure 3: Block diagram of pass logic circuit based FWFT

3.1 A Novel FWFT Method for NOMA Transmission

In order to minimize the latency in hardware implementation, this study offers an effective method with parallel approach that dramatically limited the size of iterations. Meanwhile, it performs admirably. Fig. 4 shows the complex performance of radix-4 FWFT computation. For example, one radix-4 butterfly may take up the role of up to four other radix-2 butterflies, and it only includes three complex multipliers as contrasted to the four complex multipliers required by four radix-2 butterflies. In optimal controlled, there is a low amount of real-time addition and multiplication is required in radix-4 FWFT. Optimization in FFT for speed improvement has done via the proposed radix-4 FWFT structure normally radix-2 for the higher bit length induces latency. The architecture consists of four real-number adders and two real-number multipliers, one commutator, four multiplexers, and some other components, as shown in Fig. 3. The adder for real numbers is compatible with the subtractor, real and imaginary interleave the input/output data as a result of the distance between two operators of the buffer size is described by $\frac{N}{2^{i+1}}$.
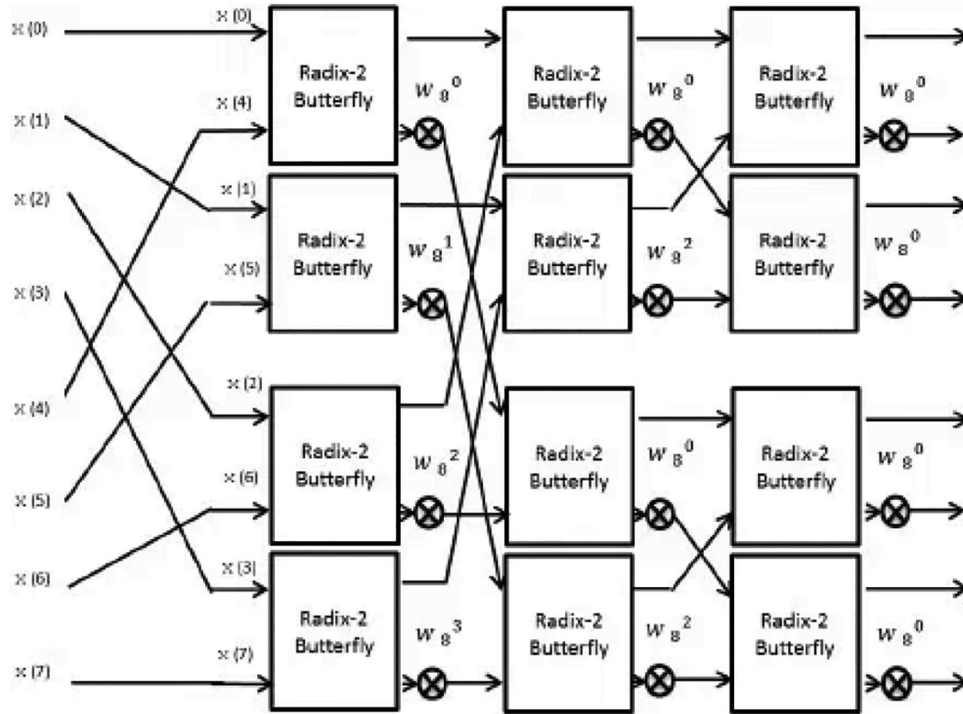
Figure 4: Radix 4 FWFT computation

Basically, an FWFT is a transform technique which is used to a pair of DFT and WHT. When compared FWFT with FFT, this method reduces complexity by log2(N)-1 and it uses FWFT to evaluate the pair of DFT and WHT. The modulated signal vector is signified as $P = [P_1, P2, P_3, \ldots, P_{N-1}]^T$ Processed by IFWFT, printed as $p = M'P$. Where $M' = \dfrac{1}{N}F' W$ is the N × N FWF-transform matrix, G & H existing S point IDFT matrix reordered in row bit inverse direction.

Then Q is retrieved from the forward FWFT process which is expressed as,

$$q = M \times Q \tag{1}$$

where $M = \dfrac{1}{S}F W$ is the forward WHT.

The column bit inverse direction changes G and H's underlying S point DFT matrix.

If IFWFT is utilized on the transmission side, the IFWFT matrices N and S can be expressed in terms.

$$M[N] = \frac{1}{N} \begin{pmatrix} T\left[\dfrac{N}{2}\right] & 0 \\ 0 & \left(\dfrac{2}{N}\right) V\left[\dfrac{N}{2}\right] W\left[\dfrac{N}{2}\right] \end{pmatrix} \tag{2}$$

We can see that M[N] is a piece transversal matrix, with two-thirds of its components having zero.

$$
M[N] = \frac{1}{N}
\begin{bmatrix}
\frac{1}{2}U[2]H[2] & 0 & 0 & \cdots & 0 & 0 \\
0 & \frac{1}{2}V[2]H[2] & 0 & \cdots & 0 & 0 \\
0 & 0 & \frac{1}{4}V[4]H[4] & \cdots & 0 & 0 \\
\ddots & \ddots & \ddots & \cdots & \ddots & \ddots \\
0 & 0 & 0 & \cdots & \frac{4}{SN}V\left[\frac{S}{4}\right]H\left[\frac{S}{4}\right] & 0 \\
0 & 0 & 0 & \cdots & 0 & \frac{2}{N}V\left[\frac{N}{2}\right]H\left[\frac{N}{2}\right]
\end{bmatrix}
\tag{3}
$$

Assume G $[2^{k+1}]$ and H $[2^{k+1}]$ keeps the IDFT matrix reordered into row inverse path then the WH matrices in size N = 2^{k+1}, accordingly. A $[2^{k+1}]$, B $[2^{k+1}]$ and H $[2^{k+1}]$ signify a sub-matrix of G $[2^{k+1}]$ and H $[2^{k+1}]$ as,

$$
G[2^{k+1}] = \frac{1}{2^{k+1}}
\begin{bmatrix}
U[2^k] & U[2^k] \\
V[2^k] & -V[2^k]
\end{bmatrix}
\tag{4}
$$

$$
H[2^{k+1}] =
\begin{bmatrix}
H[2^k] & H[2^k] \\
H[2^k] & -H[2^k]
\end{bmatrix}
\tag{5}
$$

$$
M[16] = \frac{1}{16}
\begin{bmatrix}
\frac{1}{2}U[2]H[2] & 0 & 0 & 0 \\
0 & \frac{1}{2}V[2]H[2] & 0 & 0 \\
0 & 0 & \frac{1}{2}V[4]H[4] & 0 \\
0 & 0 & 0 & \frac{1}{8}V[8]H[8]
\end{bmatrix}
\tag{6}
$$

In M [16], the sub-matrix $\frac{1}{8}$ V [8]H [8] can be written as,

$$
\frac{1}{8}B[8]H[8] =
\begin{bmatrix}
\frac{1}{8}(1+w^4)X[4]H[4] & \frac{1}{8}(1-w^4)Y[4]H[4] \\
\frac{1}{8}(1-w^4)X[4]H[4] & \frac{1}{8}(1+w^4)Y[4]H[4]
\end{bmatrix}
\tag{7}
$$

where X [4] and Y [4] can be correspondingly written as

$$
X[4] =
\begin{bmatrix}
1 & w^1 & w^2 & w^3 \\
1 & -w^1 & w^2 & -w^3 \\
1 & w^5 & -w^2 & -w^7 \\
1 & -w^5 & -w^2 & w^7
\end{bmatrix}
\tag{8}
$$

$$
Y[4] =
\begin{bmatrix}
1 & w^3 & w^6 & -w^1 \\
1 & -w^3 & w^6 & w^1 \\
1 & w^7 & -w^6 & w^5 \\
1 & -w^7 & -w^6 & -w^5
\end{bmatrix}
\tag{9}
$$

Define w = $e^{j2\Pi N}$, $Z1 = \dfrac{1+w^4}{2}$, $Z2 = \dfrac{1-w^4}{2}$, $Z3 = \dfrac{1+w^2}{2}$, $Z4 = \dfrac{1-w^2}{2}$, $Z5 = \dfrac{1+w^6}{2}$, $Z6 = \dfrac{1-w^6}{2}$,

$Z7 = 1+w\ 2$, $Z8 = 1-w\ 2$, $Z9 = \dfrac{1+w^5}{2}$, $Z10 = \dfrac{1-w^5}{2}$, $Z11 = \dfrac{1+w^3}{2}$, $Z12 = \dfrac{1-w^3}{2}$, $Z13 = \dfrac{1+w^7}{2}$ and

$Z14 = \dfrac{1-w^7}{2}$.

Then, $\dfrac{1}{2}U[2]H[2]$ and $\dfrac{1}{2}V[2]H[2]$ can be respectively obtained as

$$\frac{1}{2}U[2]V[2] = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{10}$$

$$\frac{1}{2}U[2]V[2] = \frac{1}{2}\begin{bmatrix} P2 & P1 \\ P1 & P2 \end{bmatrix} \tag{11}$$

As well, $\dfrac{1}{4}V[4]H[4]$ can be reported as

$$\frac{1}{2}V[4]H[4] = \frac{1}{4}\begin{bmatrix} 1 & w^2 & w^4 & w^6 \\ 1 & -w^2 & w^4 & -w^6 \\ 1 & w^6 & -w^4 & w^2 \\ 1 & -w^6 & -w^4 & -w^2 \end{bmatrix} \times \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix} \tag{12}$$

$$= \begin{bmatrix} Z3 & Z4 & 0 & 0 \\ Z4 & Z3 & 0 & 0 \\ 0 & 0 & Z5 & Z6 \\ 0 & 0 & Z6 & Z5 \end{bmatrix} \times \begin{bmatrix} Z1 & 0 & Z2 & 0 \\ 0 & P1 & 0 & Z2 \\ Z2 & 0 & Z1 & 0 \\ 0 & Z2 & 0 & Z1 \end{bmatrix} \tag{13}$$

$$= \begin{bmatrix} Z11 & Z12 & 0 & 0 \\ Z12 & Z11 & 0 & 0 \\ 0 & 0 & Z13 & Z14 \\ 0 & 0 & Z14 & Z13 \end{bmatrix} \times \begin{bmatrix} Z5 & 0 & Z2 & 0 \\ 0 & Z5 & 0 & Z6 \\ Z6 & 0 & Z5 & 0 \\ 0 & 6 & 0 & Z5 \end{bmatrix} \times \begin{bmatrix} Z2 & 0 & 0 & 0 \\ 0 & Z2 & 0 & 0 \\ 0 & 0 & Z2 & 0 \\ 0 & 0 & 0 & Z2 \end{bmatrix} \tag{14}$$

$$\frac{1}{8}(1-w^4)X[4]H[4] = \begin{bmatrix} Z7 & Z8 & 0 & 0 \\ Z8 & Z7 & 0 & 0 \\ 0 & 0 & Z10 & Z10 \\ 0 & 0 & Z10 & Z9 \end{bmatrix} \times \begin{bmatrix} Z3 & 0 & Z4 & 0 \\ 0 & Z3 & 0 & Z4 \\ Z4 & 0 & Z3 & 0 \\ 0 & Z4 & 0 & Z3 \end{bmatrix} \times \begin{bmatrix} Z2 & 0 & 0 & 0 \\ 0 & Z2 & 0 & 0 \\ 0 & 0 & Z2 & 0 \\ 0 & 0 & 0 & Z2 \end{bmatrix} \tag{15}$$

3.2 PL Based FWFT Realization

Fig. 6 shows the pass logic function in which the multiplication is performed with the help of the pass logic circuit. From this figure, we can clearly say that the upper part of the circuit only has an additional part, while the lower part has a multiplication with a smaller number of transistors. M Prakash et al suggested a PL circuit to decrease the number of transistors needed for operation, where the PL butterfly diagram is shown in Fig. 5. So, it consumes very little power. The result shows that the transistor controls the delay and the control transmitter for the specific power.

The normal multiplier requires more adders and shift operators to perform this function. But this is going to create the worst stage when the number of operations increases. However, in this proposed method, the 16-point radix-4 FWFT method uses PL circuits instead of multiple multipliers. As a result, requirements for hardware and capacity are significantly minimized. The range of complexity is condensed. Despite this, there is no variation in the time of implementation in the different input values.
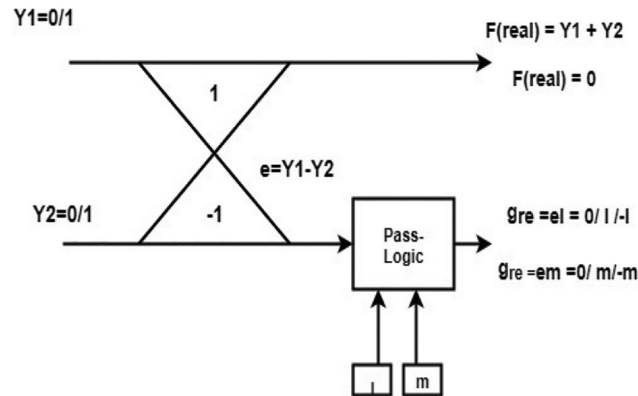
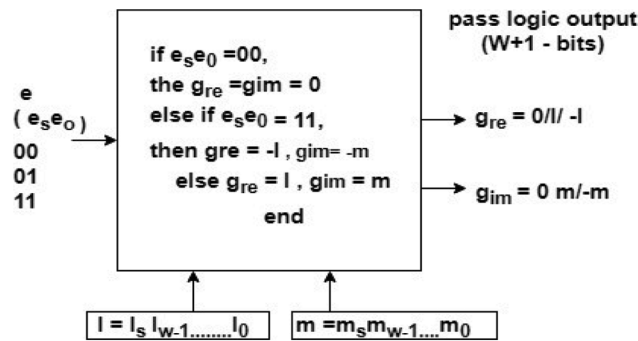**Figure 5:** PL butterfly diagram to decrease the number of multipliers

Figure 6: Pass logic circuit

When more multipliers are used, the number of gates increases, but the gate range decreases with the help of pass logic.

The Tab. 1 shows the comparison of constant multiplier and proposed PL, based on the values present in the table, we can say that the number of gates required for the constant multiplier is 48 and for PL, the required gate number is 22. If the number of gates decreased, then the size will also decrease. This has a great impact on many applications related to logic gates. But one major thing behind this concept is, it required the same time as constant multiplier need.

Table 1: Area and time comparison of proposed Pl with previous technique

Methods	Area	Time
Constant Multiplier	48	128 ps
Proposed pass logic	22	128 ps

3.3 Additional 2D DCT for BF Structure

The 2-D DCT is implemented directly from the theoretical equation, which yields 1024 multiplications and 896 additions. Fast algorithms take advantage of the DCT's symmetry to achieve significant computational savings. The discrete Fourier transform is related to the DCT in that it converts a signal from the time domain to the frequency domain. It lowers the number of memory and bandwidth needed

for digital signals dramatically. The 2-D DCT stands for two-dimensional Discrete Cosine Transform which is applicable to calculate the transform function. The common DCT equation is given as,

$$F(a,b) = \frac{2}{\sqrt{AB}} c(a)c(b) \sum_{y=0}^{A-1} \sum_{z=0}^{B-1} f(y,z) \cos\frac{(2y+1)a\pi}{2A} \cos\frac{(2y+1)b\pi}{2B} \tag{16}$$

The adder's outputs are saved in RAMs. When the WR signal is large, the write operation is performed on the corresponding RAM address. Otherwise, the RAM address's contents are read. The address signals have a length of 64 times the input clocks. Two ROMs are used to allow for continuous data writing. The outputs of the eight multipliers are then added together to produce 1D coefficient values that are saved in RAM. The intermediate RAM values are read out one column at a time (every 8th value is read out every clock), and this is the input for the 2nd DCT. The *rdy* in signal is used to communicate between the DCT and IDCT functions. When the signal is big, it tells the IDCT that the core is receiving valid data.

3.3.1 The Extra Period of 2-D DCT

$$B_1^{s_{12},s_{11},s_2}(n_2) = B_{even}^{s_{12},s_{11},s_2} + W_8^{s_2} B_{odd}^{s_{12},s_{11},s_2} \tag{17}$$

3.3.2 The Time-domain Shift Period of 2-D DCT

$$y_s[8s_1 + s_2] = W_8^{\frac{1}{4}(s_1+s_2)} . y[8s_1 + s_2] \tag{18}$$

$$\begin{aligned} X_1[8s_1 + s_2] &= \frac{1}{4}\{Re[y_s(8s_1 + s_2)] - Re[y_s(72 - 8s_1 - s_2)]\} \\ &\quad - \frac{1}{4}\{Im[y_s(64 - 8s_1 + s_2) - Im[y_s(8 + 8s_1 - s_2)]\} \end{aligned} \tag{19}$$

$$\begin{aligned} X_1[8s_1 + s_2] &= \frac{1}{4}\{Im[y_s(8s_1 + s_2)] - Im[y_s(72 - 8s_1 - s_2)]\} \\ &\quad + \frac{1}{4}\{Re[y_s(64 - 8s_1 + s_2) + Re[y_s(8 + 8s_1 - s_2)]\} \end{aligned} \tag{20}$$

$$n_1 = 4n_{11} + n_{12} \tag{21}$$

$$s_1 = 2n_{11} + s_{12} \tag{22}$$

The 2-D DCT calculation occurs and X-2 [8k-1+k-2] is determined simultaneously within the B arrangement IV post-calculation. The mathematical 8 x 8 2-D IDCT has been clarified using the process of deterioration. This reflects the triple-mode FFT/ IFFT and 2-D DCT equation to be tested as a consequence of the cost-effective imperative within the physical plan. Determination returns on the FFT/ IFFT/2-D DCT calculation based on Radix-4^2 shows that BF calculation could be effectively performed in four complicated input adders and a few trail circuits. No multipliers are used in the Radix-4 BF structure. In addition, the pair of 8 x 8 2-D DCT and 256-point FFT/IFFT pipeline procedure designs can be calculated by a standard structure. DCT is implemented using a framework called vector processing with parallel multipliers. Regular structure, easy control and interconnect, and a reasonable compromise between efficiency and complexity of implementation are all advantages of vector processing.

4 Hardware & FPGA Implementations

The described NOMA FPGA organization is executed on the USRP-RIO 2953R National Instruments SDR platform. The key benefit of this stage is the integrated Kintex7-FPGA, which enables the hosting of all

the related portions of the signal processing. The RF channels is another major benefit that provides several tools for design synthetization, formation methods, and concert investigates, including resource, speed, and power consumption. This makes a single device NOMA transceiver without the need for synchronization and data transmission with only one channel between multiple front-ends. The USRP-RIO has a frequency range of 1.2 to 6 GHz, a bandwidth of 40 MHz, and a throughput rate of 832 MB/s. The USRP is linked to a PC using the NI PXIe-PCIe8371 card. The USRP-2953 is a complete equipment / software package for quickly developing high-performance wireless communications networks. The USRP typically enables progressive waveforms to be conveniently prototyped in an occurrence series that encompasses the key bandwidths used today for portable transportations. One more major advantage of this stage is that it is possible to moderately implement the communication chain in hardware and software. Project Set is a versatile way of exploring the flexibility of SDR shared with the execution of FPGA by integrating software roles in a block group considered with a hardware description language. Researchers can design better and also get results faster with USRP RIO's combined hardware and software package. Multiple input, multiple output (MIMO); synchronization of wireless links; LTE relay; RF compression filtering; spectral sensing; cognitive radio; frequency hopping; and orientation mapping are among the important research technologies they can develop. The design process of FPGA is given in Fig. 7. After the FPGA employment, the total power and time were calculated using a power analyzer and timing analyzer based on that the consumed power and time. It is also an important part of the iterative process of optimizing FPGA performance. It can help improve/optimize timing performance and consistency. Finally, the complexity range of FWFT is compared with respect to a number of stages.
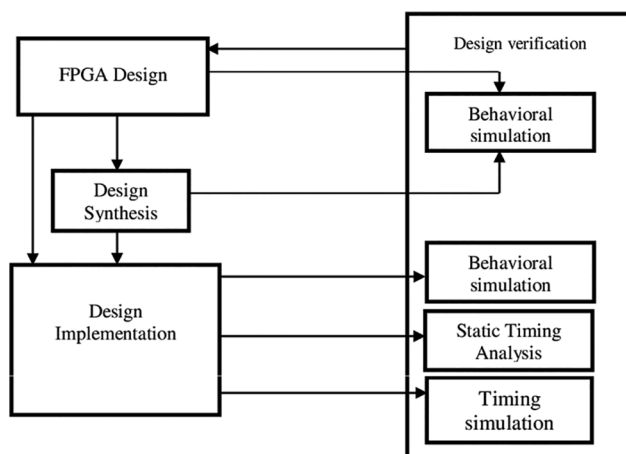

Figure 7: Design flow of FPGA

5 Experimental Results

Tab. 2 explains the comparison between FFT and FWFT. When compared with FFT, FWFT has a greater advanced related to time, area and frequency. In other previous methods, there is no pass logic and FPGA implementation were presented for the FWFT technique. Hence, this paper presents the VLSI implementation for FWFT to improve the NOMA system performance with respect to complexity and power requirement. Based on this research the complexity is reduced with the help of pass logic circuit. In previous papers, the number of transistors required for multiplication was very high and which required more power to run and designing complexity was also high. In order to avoid this problem, a novel pass logic circuit attached to FWFT is implemented.

Table 2: Comparison between FFT and FWFT

Parameters	FFT	FWFT
Technology	0.18 μ	0.18 μ
Length support	1024	2048
Voltage	1.8 V	1.5 V
Normalized area	3.89 mm^2	2.89 mm^2
Maximum frequency	128 MHz	150 MHz
Execution time	51.25 μs	35.5 μs

Tab. 3 compares some parameters for previous methods and present FWFT+FPGA method. The parameters which include internal memory, overall memory, adder, multiplier, and latency. When compared the values, we can say that, this FWFT method is better compared with other methods and the comparison of multiplier and pass logics are shown in Tab. 4

Table 3: Hardware resource comparison between the previous methods and the present method

Architecture	Internal memory	Total memory	Adder	Multiplier	Latency
R2SDC+WHT	4N-4	5N-4	$4log_2N$	$2log_4N - 1$	2N
$R2^2SDF + WHT$	2N-2	3N-2	$4log_2N$	$log_4N - 1$	3N-2
$R2^4SDF + WHT$	2N-2	3N-2	$4log_2N$	$0.67log_4N - 1$	3N-2
Proposed FWFT + FPGA	3N+2.5 $\times log_2N$-1.5	2.5 $N + 2.5 \times log_2N$-1.5	$1.5 \times log_2N$-1.5	$log_4N - 1$	$log_2N - 0.5$

Table 4: Comparison of multiplier and pass logic

Multipliers	Number of transistors	power	Delay
2×2 Multiplier	28 T	533.5184 pW	924.78 pS
2×2 Array multiplier	136 T	7.1913 nW	49.602 ns
4×4 Wallace multiplier	136 T	23.1446 nW	48.617 nS
4×4 Braum multiplier	136 T	2.6140 nW	100.56 nS
Pass logic	34 T	2.764 nW	78.256 nS

Complexity analysis: For the transmission and receipt of a given number of multi-carrier symbols, the complexity analysis of each contender is assessed as the required number of complex multiplications. Fig. 8 shows the number of complex multiplications in relation to the number of blocks. The FWFT operation is known to require a complex multiplication of $\frac{1}{2}[Nlog_2(N) - (2N - 2)]$ and a multiplication between two complex numbers requires three multiplications.

However, compared to the existing techniques, the proposed FWFT-NOMA-FPGA techniques reduce the number of complex multiplications with the help of the pass logic circuit. FBMC and GFDM are the

most effective waveforms and are five times more complex than OFDM. RB-F-OFDM and UFMC are more complex as each sub-band generates FWFT operations and is 10 times more complex than the modulated OFDM data symbol.
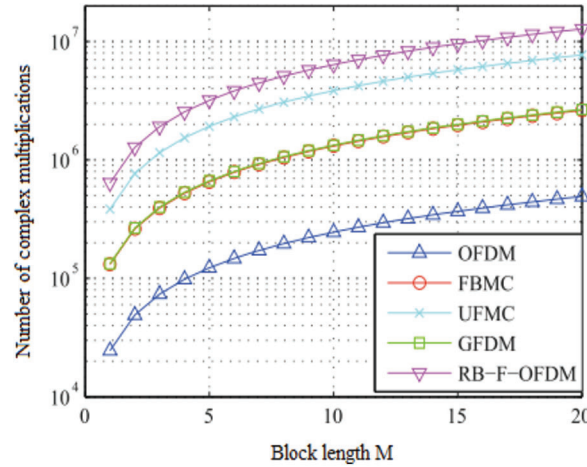

Figure 8: Block length *vs.* number of complex multiplications

A comparison of the computational complexity of the various waveform schemes is shown in Fig. 9. The complexity is quantified by the total number of actual multiplications per symbol. For the transmitter and receiver, the effect of the number of subcarriers on the complexity of waveforms has been measured and compared.
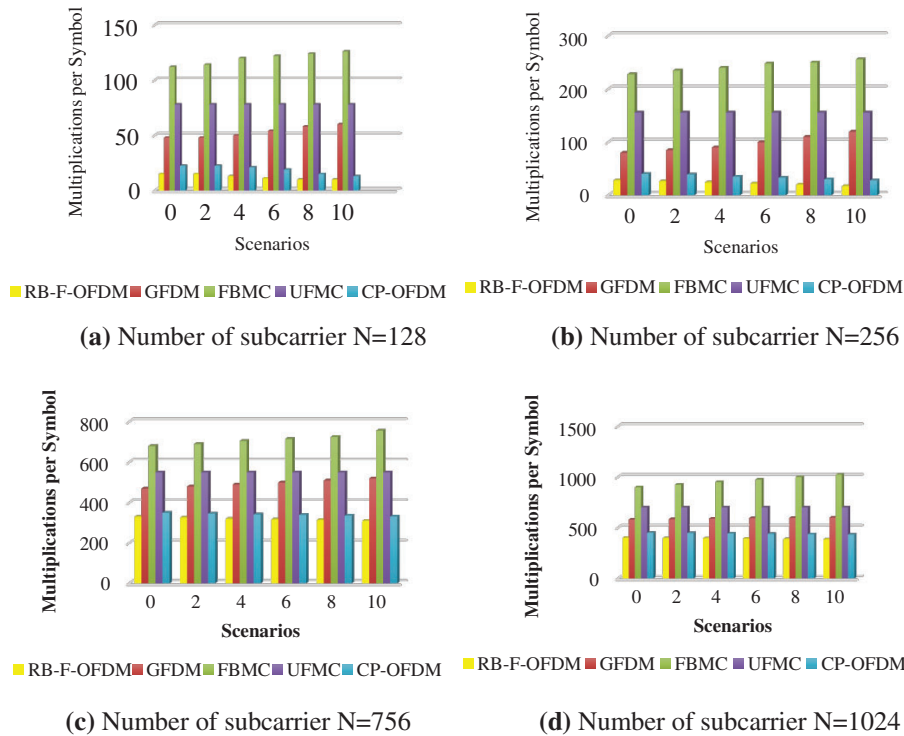

(a) Number of subcarrier N=128

(b) Number of subcarrier N=256

(c) Number of subcarrier N=756

(d) Number of subcarrier N=1024

Figure 9: Comparison of computational complexity for the various waveform schemes (a) N = 128 (b) N = 256 (c) N = 756 (d) N = 1024

Compared to existing techniques, GFDM has less than three times the number of operations, while FBMC has seven times the number of operations, and UFMC has more than nine times the number of operations. As predicted, although the simplest waveform is CP-OFDM, the more complex waveform (FBMC) shows only substantial complexity differences for N = 756 subcarriers is shown in Fig. 9c. CP-OFDM and RB-F-OFDM are two times less complex than FBMC and 1.5 times less complex than GFDM and UFMC for N = 1024 subcarriers are present is shown in Fig. 9d. For $N \geq 128$, it shows that the waveform of FBMC is more complex than the waveform of CP-OFDM is shown in Fig. 9a. Finally, the complexity performance of CP-OFDM and RB-F-OFDM is closest to OFDM and thus benefits from greater compatibility with existing systems, even though their complexity is generally lower than that of FBMC, UFMC and GFDM waveforms.

6 Conclusion

This paper presents the FPGA implementation of FWFT to make the FWFT algorithm fast and real time. With the help of FPGA and Pass logic, the proposed architecture achieves more hardware utilization and low complexity. When the FPGA was implemented, the number of transistors decreased by 21% and the total power required was reduced by 5.5%. The FPGA implementation of FWFT for 34 transistor-pass-logic customs and power consumption is 2.764 mW with a latency of 78.256 ns. As a result, the proposed system has achieved a less power, less area and low complexity system that can improve the operation of the MIMO system. Most importantly, the time requirement for the proposed methodology is very low so that it could become a promising model for the MIMO system for future 5G technology.

Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

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