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Harmonics Extraction Scheme for Power Quality Improvement Using Chbmli-Dstatcom Module

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Abstract: In recent day's power distribution system is distress from acute power quality issues. In this work, for compensating Power Quality (PQ) disturbances a seven level cascaded H-bridge inverter is implemented in distribution static compensator which protects power quality problems in currents. Distribution Static Compensator (DSTATCOM) aid to enhances power factor and removes total harmonic distortion which is drawn from non-linear load. The D–Q reference theory based hysteresis current controller is employed to generate reference current for compensation of harmonics and reactive power, additionally Probabilistic Neural Network (PNN) classifier is used which easily separates exact harmonics. In the meantime fuzzy logic controller is also used to maintain capacitor DC-link potential. When comparing to PI controller it decreases steady state time and reduces maximum peak overshoot. Cascaded H-bridge multilevel inverter converts direct current to Alternating current, through inductor opposite harmonics are injected in Power Control Centre reduces source current harmonics and reactive power. The implementation of CHBMLI in distribution STATic COMpensator simulation model is simulated by means of MATLAB.

Keywords: CHBMLI; distribution STATic COMpensator (DSTATCOM); probabilistic neural network (PNN); PI (proportional–integral); fuzzy logic control (FLC); total harmonic distortion (THD)

1 Introduction

By using DSTATCOM, harmonic relevant power quality issues are rectified. For enhancing power quality at distribution supply, a novel control system implemented on frequency adaptive disturbance observer is proposed. Furthermore, it also eliminates the harmonics from nonlinear load Power quality issues in this system are bad power factor due to loads and more neutral current due to non-linear load as well as unbalanced loads. These are overcome by notch filter based control algorithm for DSTATCOM and therefore it alleviates power quality A novel control scheme for DSTATCOM (Distribution Static Compensator) considers reactive flow control in transmission system.

It is discussed a hybrid multilevel topology based on a cascaded single phase H-bridge converter with unequal dc voltage. A diode clamped H-bridge with multi output boost rectifier performs a high voltage converter fed by DC supplies and a low voltage converter fed by DC capacitor in a high voltage inverter. The clamped diode and rectifier raise the overall cost of the system. For cascaded hybrid H-bridge converters, fundamental frequency modulation is used.

For hybrid modulation, the selective harmonic elimination method is used. For hybrid multilevel converters, a new DC voltage control strategy Delta-type cascaded hybrid single-phase H-bridge topology is preferred due to its modularity and simplicity. Probabilistic Neural Network is balancing control is accomplished by injecting zero sequence current into the delta loop, and individual voltage control is accomplished by trimming the fundamental component. Because Probabilistic Neural Network modulation does not automatically ensure that the amount of reactive power from the grid terminal is distributed uniformly among all cell capacitors, they will be charged and discharged at different rates. To avoid this undesirable situation, individual cell modulation indices must be modified from the set point provided by the outer control loop.

Because of its modularity, ability to remove the transformer in medium voltage applications, and ability to reduce switching loss, a Cascaded H-Bridge Multilevel Converter (CHB-MC) is one of the most popular converter systems in many industrial applications. Although the CHB-MC has these benefits, the requirement for isolated DC power sources, which makes the system heavy, complex, and adds cost to each HB cell, is a disadvantage to consider. In the static synchronous compensator application, however, the requirement for isolated DC power sources is no longer a significant disadvantage because floating capacitors on the HB cells can replace the isolated DC sources.

Each cell has an isolating electrolytic capacitor. An inductor is also used in each cluster to support the difference between the sinusoidal source voltage and the ac pulse width modulation voltage, as well as to filter out switch ripples caused by high frequency modulation. Switching frequencies are assigned to high voltage converters and low voltage converters, respectively. The STATCOM control scheme is tasked with generating the desired amount of reactive power at the grid terminal while keeping the mean value of the cell capacitors' voltage at a constant level. The top-level control is made up of two loops, as shown in the diagram below.

In distant region a number of distributed power generation systems are present. By using composite observer DSTATCOM is performed by means of induction generator based distributed power generation. The advantages of this scheme reduces cost, separate DC source is not required, when comparing to synchronous generator excitation current is less, maintenance is simple. This kind of scheme is only fit for portable isolated power generation system [1]. For enhancing power quality, the combination of least mean square-least mean fourth based control algorithm of distribution static compensator is developed. The issues in load balancing and power quality are overcome by this algorithm. The advantages of this control algorithm aid in faster as well as precise response with a vigorous design and convergence speed is also faster. By choosing either Least Mean Square (LMS) or Least Mean Fourth (LMF) generated pulse the error is reduced which helps in the operation of DSTATCOM [2]. DC-link potential regulation is attained by means of Reduced Switch Reduced Switch Count Multilevel Converter (RSC-MLC). The preferred range of DC-link potential is acquired in this converter which operates by using PWM technique. The advantages of this technique are it reduces potential stress, switching loss [3].

Under the state of light load, for maintaining constant DC potential needless potential stress occurs on switching devices. To overcome this drawback a dynamic DC potential regulation is suggested, it minimizes potential stress occurs on switching devices under the state of minimized load [4]. An active control for 3Φ two level DSTATCOM (Distribution Static Compensator) is proposed. The problems in power quality are overcome by this control scheme. Advantages of this scheme are static error present is less, attains faster convergence, it also enhances the power qualities like compensation on harmonics, voltage regulation, power factor correction etc. [5]. An adaptive neural network based control technique is instigated for synchronous reluctance generator to enhance power quality issues like harmonics, balanced load and potential control [6]. The PV control scheme as DSTATCOM is employed which is operated by means of combined Active Current Control (ACC) and Feed-Forward Control Loop (FFCL) arrangement is efficiently computable and unconditionally stable [7].

For improving transient behavior of Static Synchronous Compensator (STATCOM) a novel reactive current reference algorithm is proposed. The proposed algorithm improves transient behavior of closed-loop scheme among PI controller & reduces STATCOM reactive current ripples [8]. Under ordinary operating mode load reactive power compensates which developed in DSTATCOM allows the dynamic reference load voltage generation system [9]. Some of the issues in power quality are harmonics, unbalanced loads and voltage regulation. These are overcome by a novel method called affine projection control algorithm [10]. A novel algorithm of JAYA optimization method is proposed to find gain of proportional integral controller. The behavior for design contains removal of harmonics and power factor enhancement. Moreover, this system is not affected due to any change in load [11].

To compensate current relevant power quality problems Model Predictive Control (MPC) of Three-Phase Split Capacitor (TPSC) distribution static compensator with VIKOR technique is developed. The drawback of MPC is it has higher switching frequency. To mitigate this issue, one control is to repress potential divergence as well as another one minimizes switching frequency that involves cost function using weighting factors [12]. In [13] Distribution static compensator aid induction generator is instigated with sliding mode controller along with PI (Proportional Integral) controller algorithm for alleviating power quality issues and improving the ability of active power in generator. Enhanced behavior interactive DSTATCOM is proposed, that works in current control mode to alleviate current relevant Power Quality (PQ) issues [14]. A grid control tied smart photo voltaic distribution static compensator by means of adaptive RZA control algorithm is proposed which enhances power quality and helps 3Φ AC network by giving power to both network as well as loads [15].

The output of DSTATCOM (Distribution Static Compensator) is Steady state which is obtained in reactive flow control. At distribution side power quality issues are harmonics, reactive power and unbalanced load. To overcome this drawback an immune feedback control algorithm for 3Φ DSTATCOM is proposed. This control algorithm proposed in DSTATCOM keeps load balanced and eliminates harmonics. Mitigation of power quality problems are instigated by using kernel incremental metal earning algorithm in DSTATCOM the drawbacks of DC-link potential overshoot and increase in time of DC-link potential is overcome by a double deadbeat-loop control scheme for DSTATCOM is presented. Advantages in this method are transient response is faster, design process is easy and less steady-state A novel application of Multiple Complex Coefficient Filter (MCCF) is presented. This filter removes harmonics and necessary elements on nonlinear load current A VFFRLS (Variable Forgetting Factor Recursive Least Square) based control scheme is suggested for distribution static compensator. The proposed control algorithm alleviates power quality issues namely harmonics, reactive power and unbalanced load by means of the proposed AVSF algorithm is instigated for distribution static compensator. This algorithm alleviates power quality problems are harmonics, enhances power factor under linear & non-linear load.

This work presents a seven level cascaded H-bridge inverter based DSTATCOM is employed to protect power quality problems in currents. DSTATCOM aid to enhance power factor and then it removes total harmonic distortion which is supplying from non-linear load. D–Q reference theory based hysteresis current controller is employed to generate reference current for the compensation of harmonics and reactive power, additionally Probabilistic Neural Network (PNN) classifier is used which easily separates exact harmonics. For keeping constant DC-link capacitor potential, Fuzzy logic control (FLC) is used. This controller decreases steady state time and reduces maximum peak overshoot. The Cascade H-Bridge Multilevel Inverter (CHBMLI) converts DC to AC, through inductor opposite harmonics are injected in PCC reduces source current harmonics and reactive power.

2 Proposed System

The block diagram of proposed 3Φ seven level cascaded H- bridge inverter is depicted in Fig. 1. This block diagram consists of 3Φ AC source, D–Q theory & PNN classifier, **Pulse-width modulation** generator, fuzzy logic controller and non-linear load.

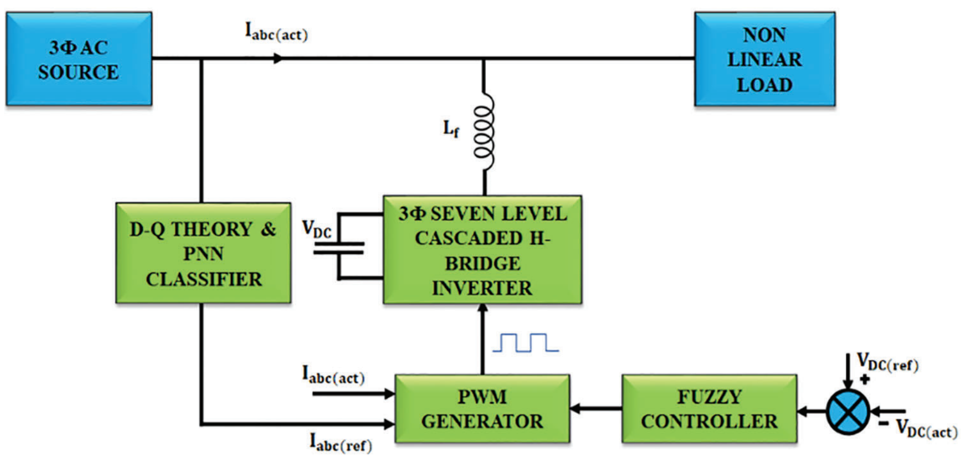

Figure 1: Block Diagram of proposed 3Φ seven level cascaded H-bridge inverter

A 3Φ AC supply is fed to linear and non-linear load. This non-linear load consists of inductance, capacitance as well as diode bridge rectifier. Due to these non-linear loads back **Electromotive Force** is produced and harmonic problems are created in source current. So real power increases and reactive power decreases. To overcome these problems DSTATCOM is used. Generally, conventional two level inverter is used in DSTATCOM this inverter increases the THD. So seven level inverter is used, for reducing the losses in seven level inverter cascaded type inverter is used. By using CHBMLI it reduces total harmonic distortion but this CHBMLI will inject opposite harmonics to PCC through inductor. Therefore, from source current it is given to D–Q theory to find out how much opposite harmonics are injected.

In DQ theory, the direct axis and quadrature axis component are determined by means of parks and clarks transformation. From this the exact harmonics are separated by means of PNN classifier. This classifier generates reference current and by using this classifier harmonics present component and pure component are determined. Meantime DC-link potential is connected in capacitor bank. For maintaining constant DC-link voltage, reference DC potential and actual DC potential are compared to fuzzy logic controller. Conventionally there is PI controller; drawbacks in PI (Proportional–Integral) Controller are it increases steady state time and maximum peak overshoot problems.

To overcome this issues fuzzy logic controller is used, this FLC decreases all problems. When comparing reference voltage, $V_{DC(ref)}$ and actual voltage $V_{DC(act)}$ in fuzzy logic controller reference current is obtained and so there is no harmonics in this reference current. Therefore, this current is merge to i_{ds} and then given to PWM generator. The working of PWM generator is, the generated reference current $I_{abc(ref)}$ i.e., from DQ theory to PNN as well as actual current $I_{abc(act)}$ i.e., source current are compared and then remaining pulses are fed to hysteresis current controller. The working of hysteresis current controller is it generates Pulse-Width Modulation (PWM) pulse and this pulse is given to seven level inverter. This inverter converts DC to AC. Through inductor opposite harmonics are injected to Power Control Center (PCC) and therefore in source current harmonics decreases, indirectly real power increases and reactive power decreases.

3 Modeling of Proposed Seven Level Cascaded H-bridge Inverter

The structure of cascaded H-bridge multilevel inverter contains $(m-1)/2$ cascaded cells in every phase as shown in Fig. 2. Every cascaded H-bridge multilevel inverter needs capacitor DC-link potential for generation of AC output potential. The output DC potential as well as AC potential system equations are represents in Eqs. (1)–(4). CHBMLI bandwidth is decided based on higher level of harmonics for compensation in DSTATCOM. For system implementation, increased level of inverters is needed in CHBMLI which have linear relationship among number of H-bridge cells as well as DC-link capacitor potential. However, enhancement in potential outcome behavior didn't pursue linear relations and therefore there is no improvement in behavior of increased level of inverters. A seven level cascaded H-bridge inverter is employed for implementation of system at a medium voltage of (415–1100 V). Every H- bridges are linked in cascade will generates potential of $+V_{dc}$, 0 and $-V_{dc}$.

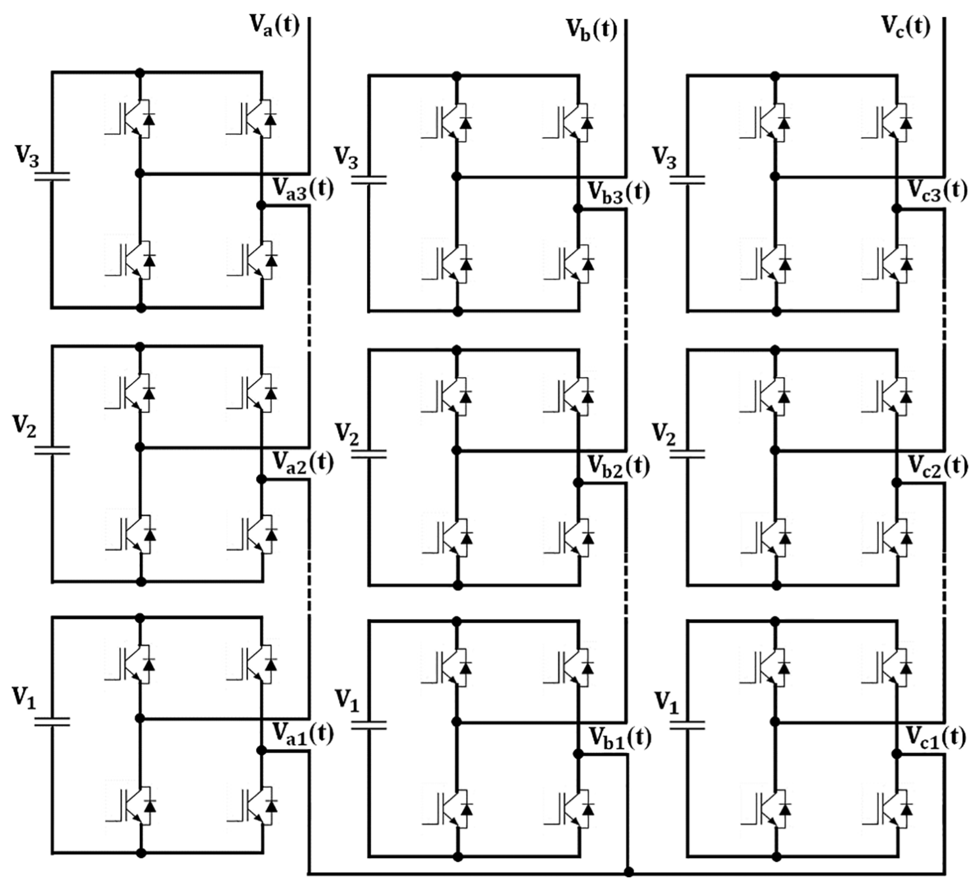

Figure 2: Structure of 3Φ seven level cascaded H- bridge inverter

The output voltage per phase for maximum value is represented as,

$$V_a = V_{aH1} + V_{aH2} + \cdots + V_{aH[(m-1)/2-1]} + V_{a[(m-1)/2]} \quad (1)$$

By presuming every H-bridge has an equal DC bus potential, i.e., $V_{aH1} = V_{aH2} = \cdots = V_{aH[(m-1)/2-1]} = V_{a[(m-1)/2]} = V_{dc}$

The CHBMLI output potential is too represented as,

$$V_A(\omega t) = \sum_{n=1}^{n=\infty} f(x, n)(\sin n\omega t) \quad (2)$$

where,

$$f(x, n) = \frac{4V_{dc}}{n\pi} \sum_{k=1}^{(m-1)/2} (a_n \, cosn\alpha_k) \quad (3)$$

Just like that the essential switching angles to be restricted are,

$$\frac{\pi}{2} > \alpha_m > \cdots \alpha_2 > \alpha_1 \quad (4)$$

4 Implemented System

The following diagram represents shunt connected DSTATCOM which is implemented in 3Φ seven level cascaded H-bridge inverter as depicted in Fig. 3.

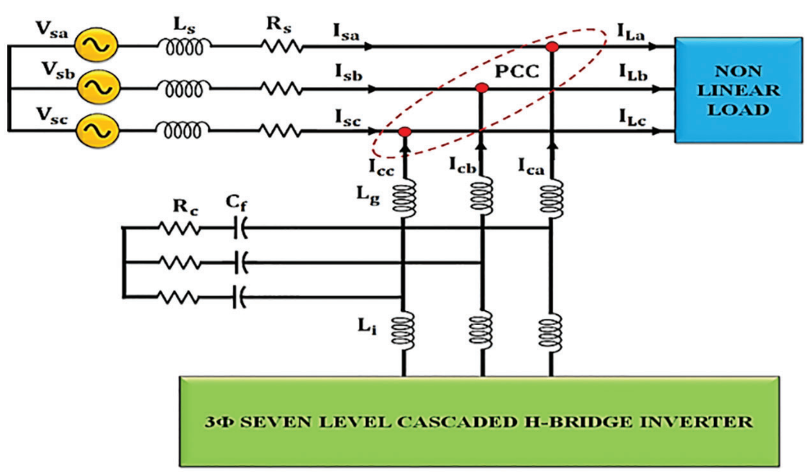

Figure 3: Shunt connected distribution static compensator

A 3Φ seven level cascaded H- bridge inverter based distribution static compensator is implemented in this scheme. When comparing to previous inverter more gate signals are needed, however one of the most important benefit of proposed method is it reduces total harmonic distortion. The application of control scheme is this inverter produces VSI and therefore this voltage source inverter generates an AC which is in phase with supply potential. The waveform for potential in every phase of seven-level cascaded inverter contains seven leveled outputs with three H-bridges linked in cascade. Through coupling inductance every phase voltage is given to distribution lines, this form shunt connected distribution static compensator. From above diagram we know that V_{sa}, V_{sb} and V_{sc} are source phase voltages which is linked to non-linear load, per phase line inductance is denoted as L_s, per phase load currents are I_{La}, I_{Lb} and I_{Lc} are denoted as per phase load currents. Kirchoff's Current Law is easily applied at the point of coupling because CHBMLI is connected in shunt arrangement.

The design of DSTATCOM with dissimilar parameter analyzes the reactive power as well as harmonic compensation. From the source it draws lagging, leading, harmonic distortions as well as unbalancing load currents which are connected to linear, non-linear and unbalanced load. The performance of compensation in reactive power and harmonics are performed in shunt connected device and distribution static compensator provides current component also preventable.

The current equation is mathematically represents in Eq. (5). The current compensation is needed for the enhancement of power quality which is generated by shunt device. This outcome of source current is sinusoidal at the region of PCC.

$$\begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} = \begin{bmatrix} I_{Ca} \\ I_{Cb} \\ I_{Cc} \end{bmatrix} + \begin{bmatrix} I_{sa} \\ I_{sb} \\ I_{sc} \end{bmatrix} \quad (5)$$

a. Reference Current Theory For CHMLI

The basic block diagram of reference current generation is depicted in Fig. 4, which is responsible for compensation of reactive power and harmonics.

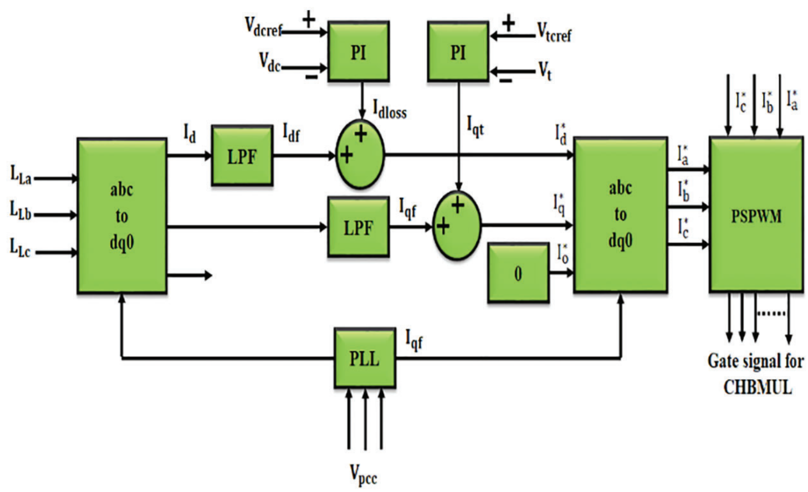

Figure 4: Block diagram of reference current generation for indirect current control

The direct axis and quadrature axis current is needed for real and reactive power in this control scheme. The fundamental current component is obtained due to load current of low pass filter. Hence it requires only active power from the source otherwise it requires average DC component $(I_d{}^*)$ from grid. Owing to charging and discharging of capacitors a small quantity of real power is absorbed by distribution static compensator and so certain losses are acquired in grid owing to current component. The inverter losses are compensated by capacitor DC voltage and therefore it requires current to keep capacitor DC-link potential which is further connected to real power.

The mathematical expression for transformation of current from *abc* to *dq*0 axis and *dq*0 to *abc* axis transformation are,

$$\begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \omega t & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ -\sin \omega t & -\sin\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} \tag{6}$$

The inverse transformation from *dq*0 to *abc* phases can also expressed as,

$$\begin{bmatrix} I_a{}^* \\ I_b{}^* \\ I_c{}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \omega t & -\sin \omega t & \frac{1}{\sqrt{2}} \\ \cos\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t - \frac{2\pi}{3}\right) & \frac{1}{\sqrt{2}} \\ \cos\left(\omega t + \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} I_d{}^* \\ I_q{}^* \\ I_0{}^* \end{bmatrix} \tag{7}$$

Generally, the reference current for indirect control is evaluated by means of terminal voltage, V_t

$$V_t = \sqrt{\frac{2}{3}\left(V_{sa}{}^2 + V_{sb}{}^2 + V_{sc}{}^2\right)} \tag{8}$$

$$I_{qt} = K_p\left(V_{tref} - V_t\right) + K_i\left(V_{tref} - V_t\right) \tag{9}$$

$$I_d{}^* = I_{df} + I_{d,loss} \tag{10}$$

$$I_q{}^* = I_{qf} + I_{q,t} \tag{11}$$

where, the terminal voltage of PCC is denoted as V_t which is regulated by proportional integral controller to keeps power quality by considering disturbances of voltage sag and swell.

5 Probabilistic Neural Network

The structure of PNN is depicted in Fig. 5. For categorizing Power Quality (PQ) disturbances, a probabilistic neural network of three layer model is required for classifier. The compose of feature vector $\vec{F}$ is chosen as PNN classifier inputs are $v_1,\ v_2,\ v_3$ and v_4 as well as nine kinds of Power Quality (PQ) disturbances are denoted as $c_1,\ c_2,\ \ldots,\ c_9$.

The features are removed by Trager Energy Operator (TEO) and OCSe compose of feature vector which is considered as PNN input. Transient features of Power Quality (PQ) disturbances are removed by OCSe. TEO reflects energy signals.

The compose of feature vector, $\vec{F}$ which consists of OCSe and TEO, is expressed as,

$$\vec{F} = [v_1,\ v_2,\ v_3, v_4] \tag{12}$$

where,

$$\begin{cases} v_1(m) = \dfrac{1}{p}\displaystyle\sum_{m=k}^{k+p}\{OCSe(m)\}; \\ v_{2\,(m)} = \sqrt{\dfrac{1}{p-1}\displaystyle\sum_{m=k}^{k+p}\left(OCSe(m) - v_1\right)^2}; \\ v_{3\,(m)} = \dfrac{1}{p}\displaystyle\sum_{m=k}^{k+p}\{|A(m)|\}; \\ v_4(m) = \sqrt{\dfrac{1}{p-1}\left(\displaystyle\sum_{m=k}^{k+p}\left(|A(m)| - v_3\right)^2\right).} \end{cases} \tag{13}$$

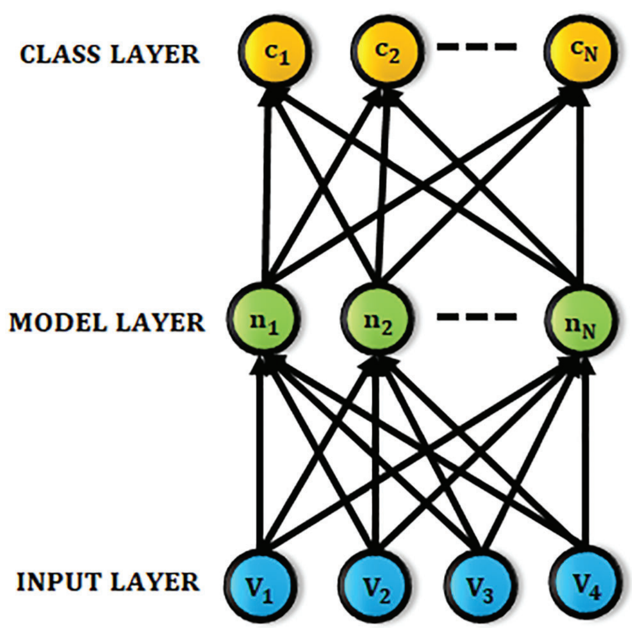

Figure 5: Structure of probabilistic neural network

Here, classification of window length is denoted as p this lays at 1/4 cycle, absolute amplitude of $f(m)$ is denoted as $|A(m)|$.

The steps involved in PNN trained are,

Step 1: The nine kinds of Power Quality (PQ) disturbances of feature vectors are attained and this is used as probabilistic neural network input. The disturbances obtained in parameters are duration, magnitude and time Constance which is selected within the limit value. Here, for every kind of signal disturbances 20 training samples are used in this work and therefore totally 20 × 9 = 180 training samples are attained.

Step 2: The following step is considered as feature vectors which composed the matrix of probabilistic neural network input. The compose of feature vector, $\vec{F}$ stated that every feature vector composes PNN input as 9 × 20 matrix.

Step 3: Probabilistic neural network is adopted and trained with parameter h_n. After the conversion of vector, a class vector of probabilistic neural network indicate 1 × 9 matrix that resembles nine kinds of power quality signal disturbances. So this probabilistic neural network trained by means of 180 samples, so this proposed probabilistic neural network is used to categorize power quality disturbances.

6 DC Link Capacitance Voltage

A seven level cascaded H-bridge inverter is employed in DSTATCOM. It contains three H-bridges in every phase, three capacitors per phase and totally nine capacitors in seven level cascaded H-bridge inverter based DSTATCOM. For complete operation voltage across every capacitor is maintain balanced. Several methods are used to balance voltage across DC-link capacitors.

6.1 PI Controller

Conventionally PI controller is used, here steady state time increases. To overcome this limitation, FLC is used to keeps DC-link potential. In this method steady state time decreases. The equation for cascaded H-bridge DC capacitance is expressed as,

$$C_{dc-cascaded} = \frac{I_{rms} \times 100}{\sqrt{2}\pi f_g \% V_r V_{dc}} \left[1 - \sin\left(arcos\left(\frac{M\pi}{4}\right)\right)\right] \tag{14}$$

where, **root-mean-square** load current for rated value is denoted as I_{rms}, system supply frequency is denoted as f_g, ripple voltage for peak-to-peak value is denoted as V_r, bus voltage for DC is denoted as V_{dc}, Modulation Index is denoted as M. The voltage across every phase is equal, and if it is not equal this is attained by means of individual voltage balancing method. The proportional integral (PI) controller it is used due to simplicity, applicability and easy control. Owing to charging and discharging, power losses in capacitor current i_{dloss} is mathematically expressed as,

$$i_{dloss} = K_p\left(V_{dcref} - V_{dc}\right) + K_i\left(V_{dcref} - V_{dc}\right) \tag{15}$$

This is the equation for proportional integral controller, this operates the system with capacitor potential will be equal to reference of DC link potential V_{dcref}. Across every bridge nine PI controllers are used in proposed feedback control loop.

6.2 Fuzzy Logic Controller

Proportional integral controller has some drawback which is incapability to respond sudden changes in error signal (e), so it is ineffective in nonlinear process. FLC is employed to overcome these drawbacks hence it is more efficient in nonlinear process. The block diagram of FLC (Fuzzy Logic Control) is depicted in Fig. 6. It contains russification, rule base fuzzy control, defuzzification, and inference engine.

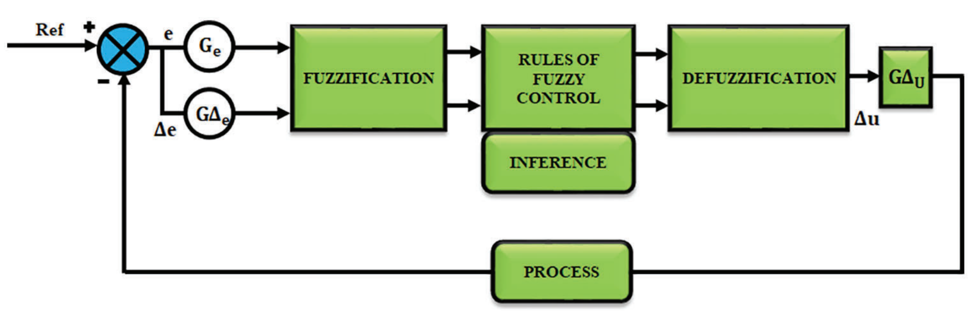

Figure 6: Block diagram of fuzzy logic controller

The control signal output is obtained from inference engine by means of rule base fuzzy control having if-then rules. By means of rule base fuzzy control, error signal (e) value, and change in error (Δe) value is changed according to output value. By using trial and error method the structure and determination of rule base is obtained.

Mathematical equation for error signal and change in error signal is expressed as,

$$\begin{Bmatrix} e_k = Y_{ref} - Y_k \\ \Delta e_k = e_k - e_{k-1} \end{Bmatrix} \tag{16}$$

Generally, the membership function presents one for every variable as three, five or seven sets. In this work seven sets are selected for representation of membership function in triangular form. Seven kinds of standard sizes in universe of speech are represented in Fig. 7.

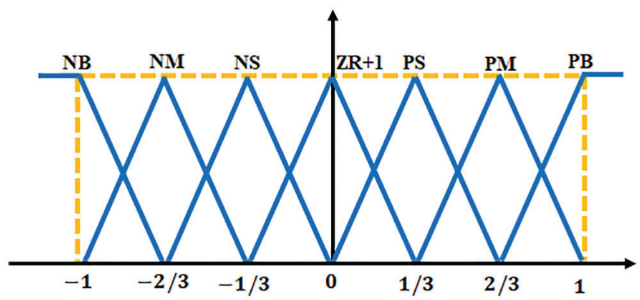

Figure 7: Distribution of function of membership in triangular form

The value used in sets which depends on resolution and intervention of preferred modification. Generally, more than seven sets don't have any improvement in dynamic performance of fuzzy logic.

7 Results and Discussion

This work clearly explains the working of proposed DSTATCOM topology using 3Φ seven level cascaded H-bridge inverter. This complete topology is developed in MATLAB simlink which is examined for linear as well as non-linear load. Here, cascaded H-bridge multilevel inverter based distribution static compensator operation as well as component design are presented. Different kinds of voltage and current waveforms are shown below representing total harmonic distortion.

A 3Φ source voltage AC waveform is depicted in Fig. 8. This AC supply is given to linear and non-linear load. Owing to non-linear load this potential is affected by means of harmonics. By using proposed DSTATCOM it minimizes harmonics.

A 3Φ source current waveform is depicted in Fig. 9. Owing to lenz's law, back EMF from non-linear load is highly affected source potential as well as current. So these problems are rectified by means of proposed reference current theory. The harmonics present in the source current are reduced by means of reference current theory based hysteresis current controller.

The DC link capacitor potential waveform is depicted in Fig. 10. By using PI controller capacitor DC-link voltage maintains near to constant voltage. In this PI controller steady state time increases and maximum peak overshoot occurs in output potential. To overcome this drawback fuzzy logic controller is used.

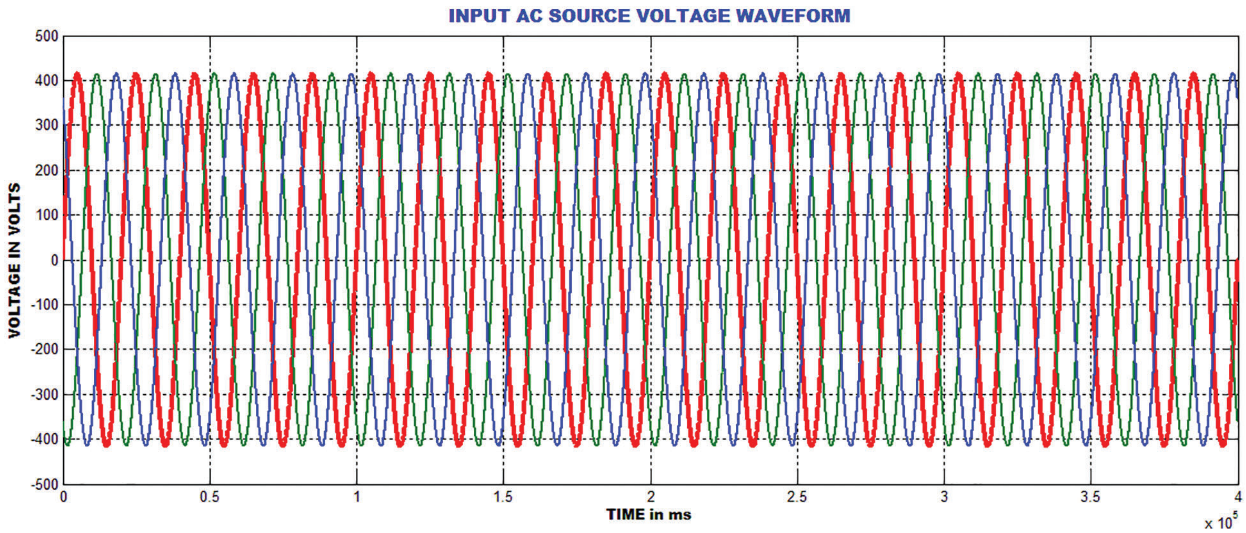

Figure 8: Three phase source voltage waveform

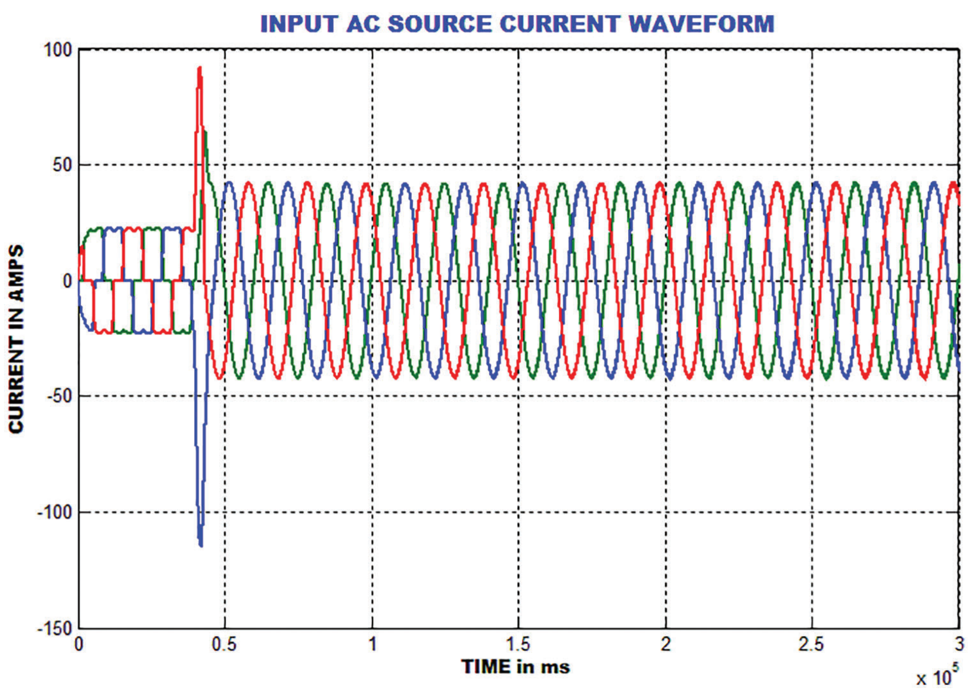

Figure 9: Three phase source current waveform

The DC link capacitor potential waveform using FLC is depicted in Fig. 11. For maintaining DC-link capacitor potential constant, mamdani method is used in FLC. When comparing to proportional integral controller, this controller reduces the settling time as well as maximum peak overshoot. A 3Φ AC current waveform is depicted in Fig. 12 is injected in PCC, current in PCC keeps sinusoidal by means of D–Q theory. A 3Φ AC voltage waveform in PCC is depicted in Fig. 13. Voltage in PCC keeps sinusoidal by means of D–Q theory.

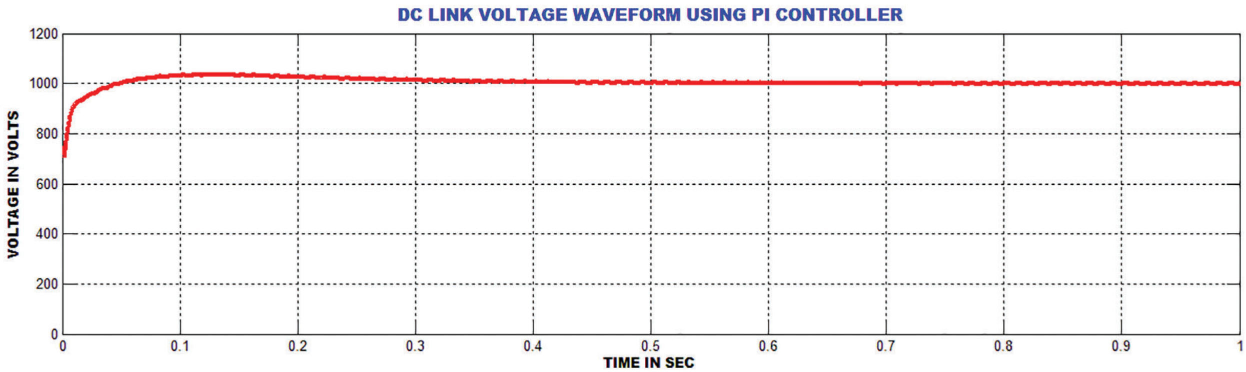

Figure 10: DC link voltage waveform using PI controller

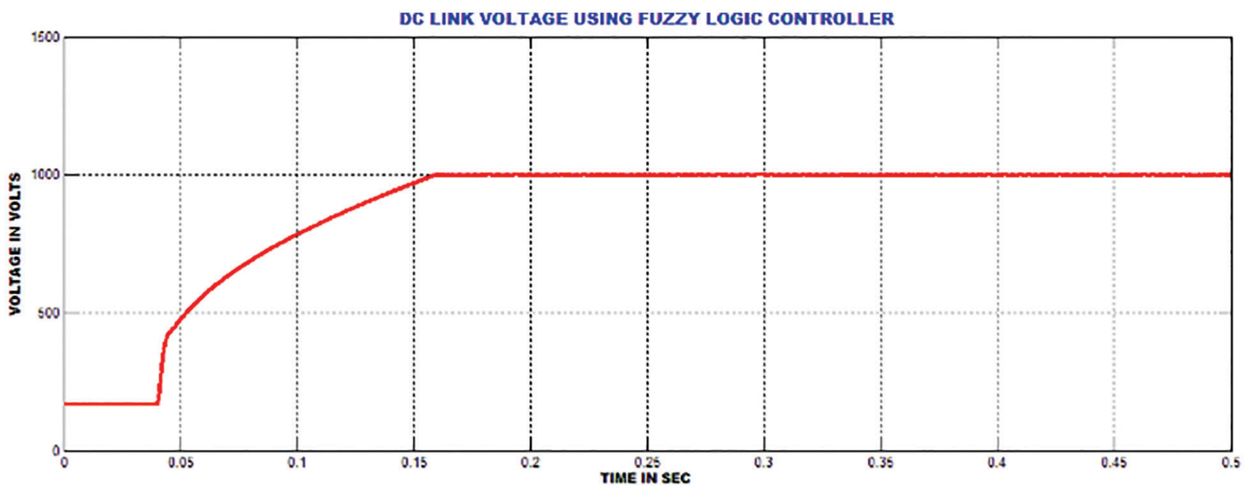

Figure 11: DC link voltage waveform using fuzzy logic controller

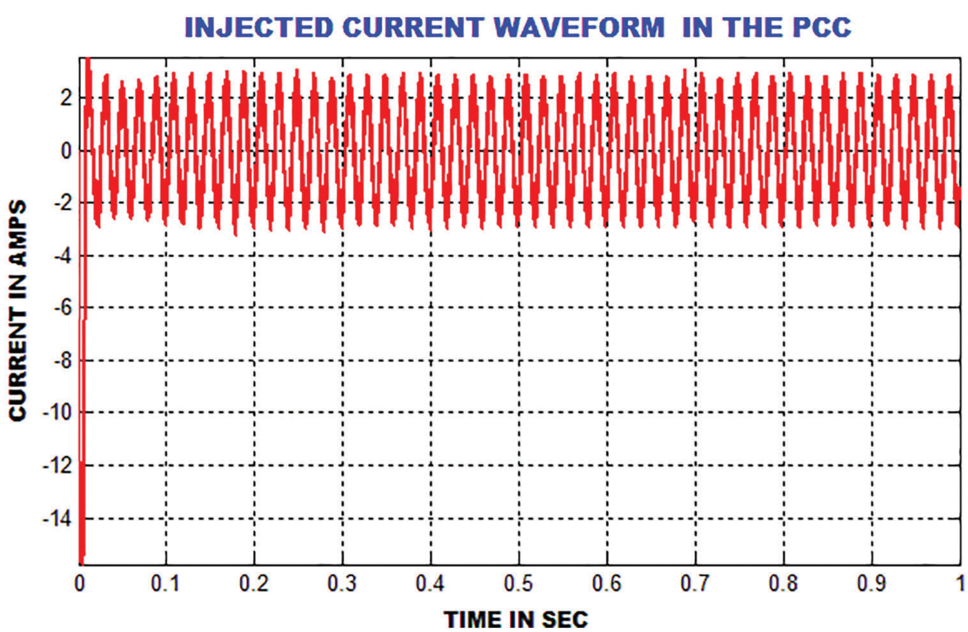

Figure 12: Current waveform injected in PCC

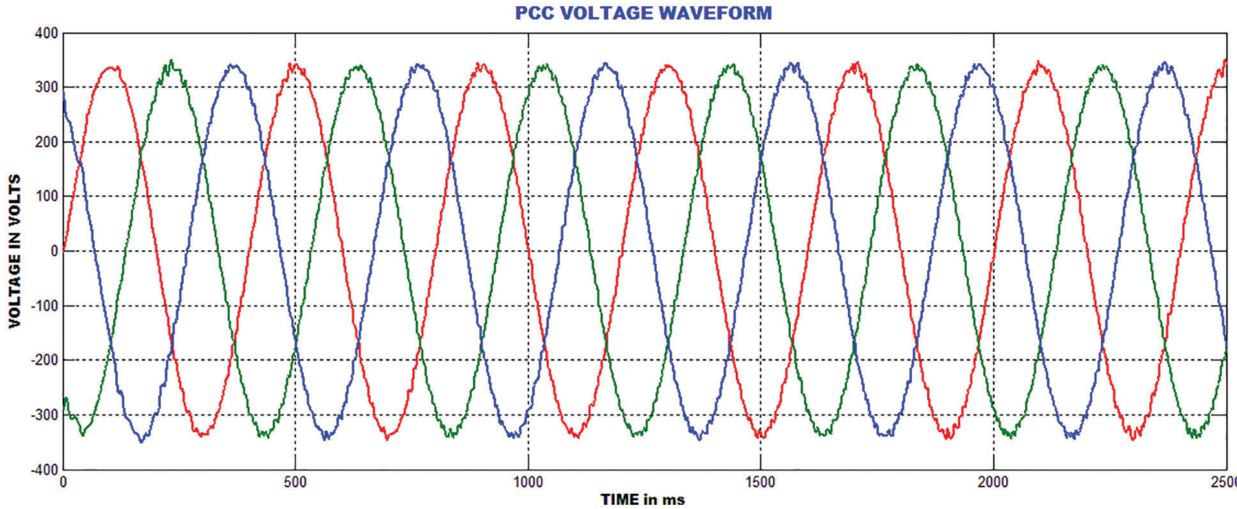

Figure 13: Three phase AC voltage waveform in PCC

A 3Φ AC current waveform in PCC is depicted in Fig. 14. By means of D–Q theory, in PCC this keeps current in sinusoidal nature. A 3Φ load voltage AC waveform is depicted in Fig. 15. Power quality issues in non-linear load are rectified by means of D–Q theory as well as fuzzy logic controller. A 3Φ load current AC waveform is depicted in Fig. 16. By using hysteresis current controllers the power quality issues are minimized. In output side, the load current waveform attains sinusoidal. Consequently, this scheme minimizes supply potential as well as total harmonic distortion current.

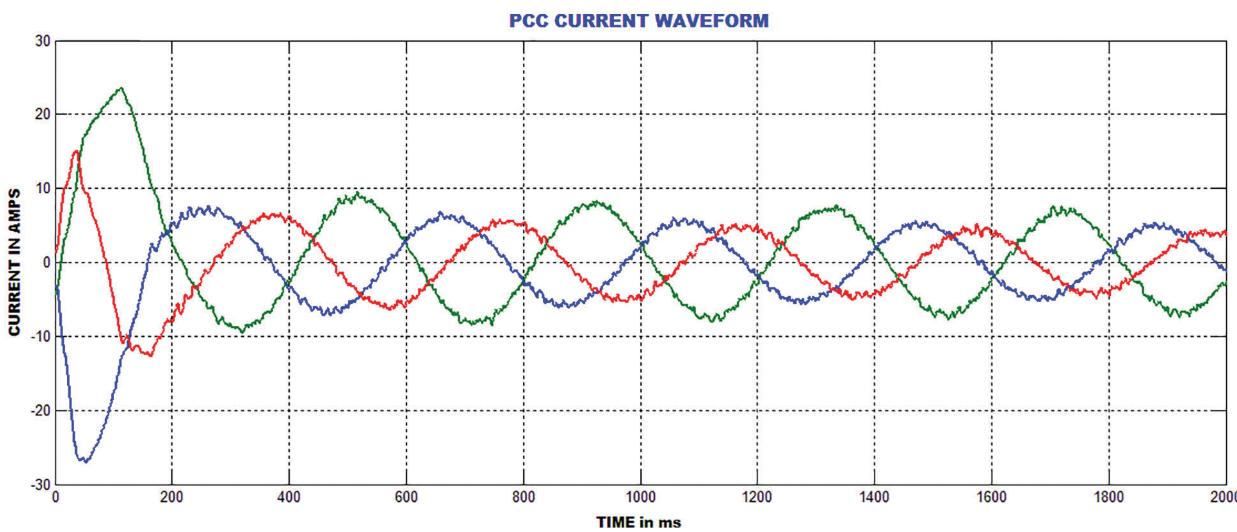

Figure 14: Three phase AC current waveform in PCC

The Source voltage and current total harmonic distortion waveform using proportional integral controller is depicted in Figs. 17 and 18. Maximum peak overshoot issues are attained in PI controller. The supply current as well as potential harmonics are high in PI controller. So, these issues overcome by FLC. This controller minimizes harmonics in source voltage and current.

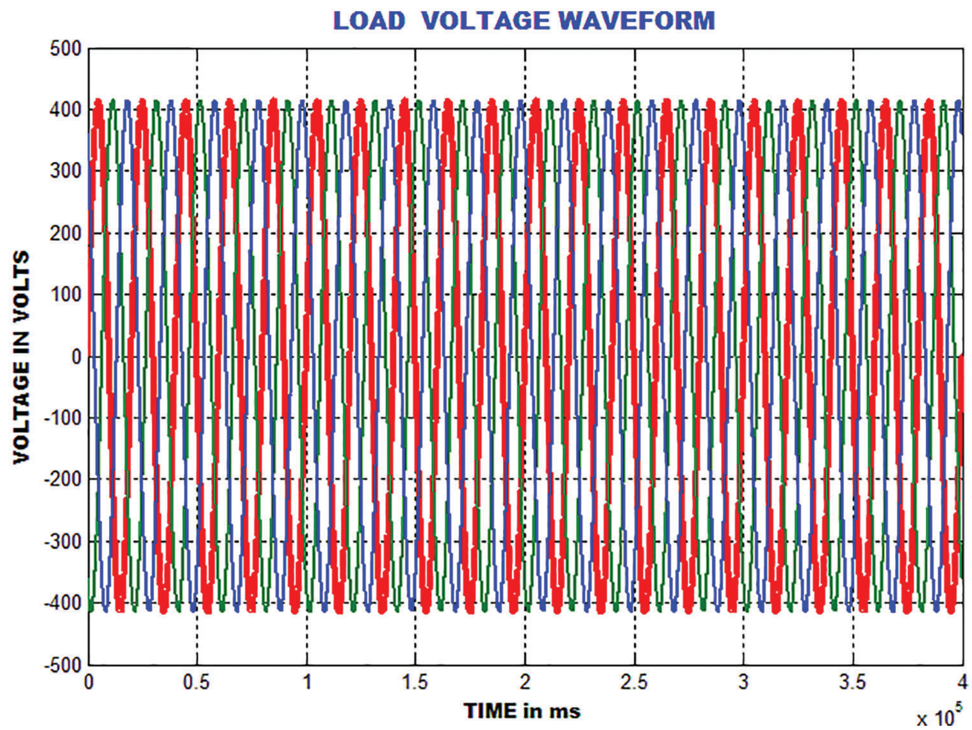

Figure 15: Three phase load voltage waveform

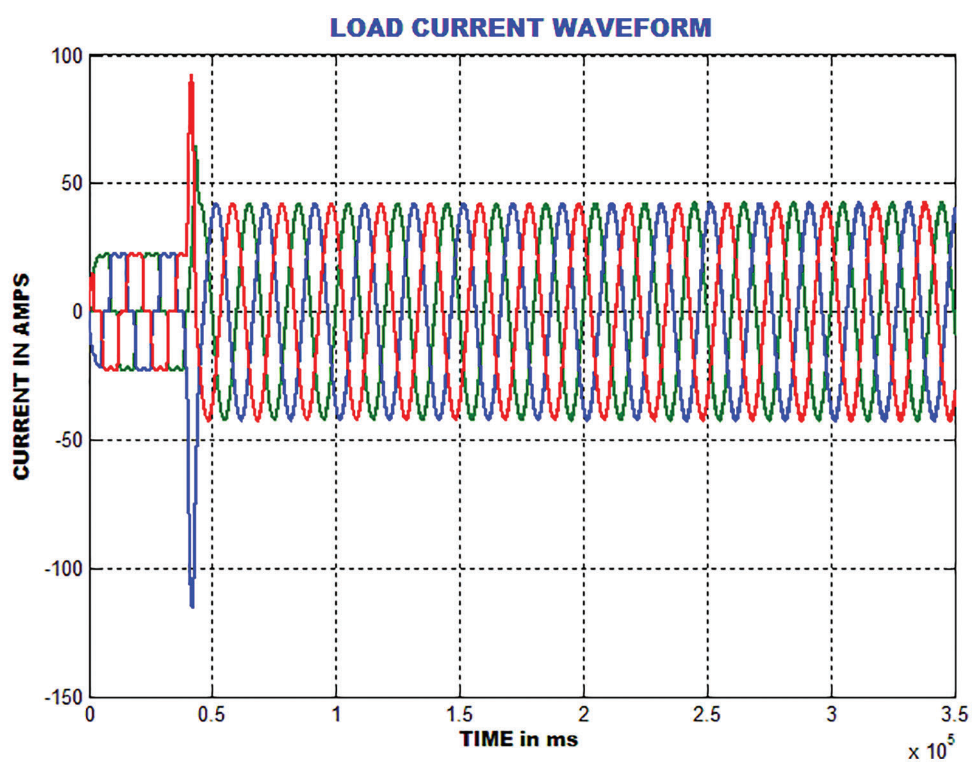

Figure 16: Three phase load current waveform

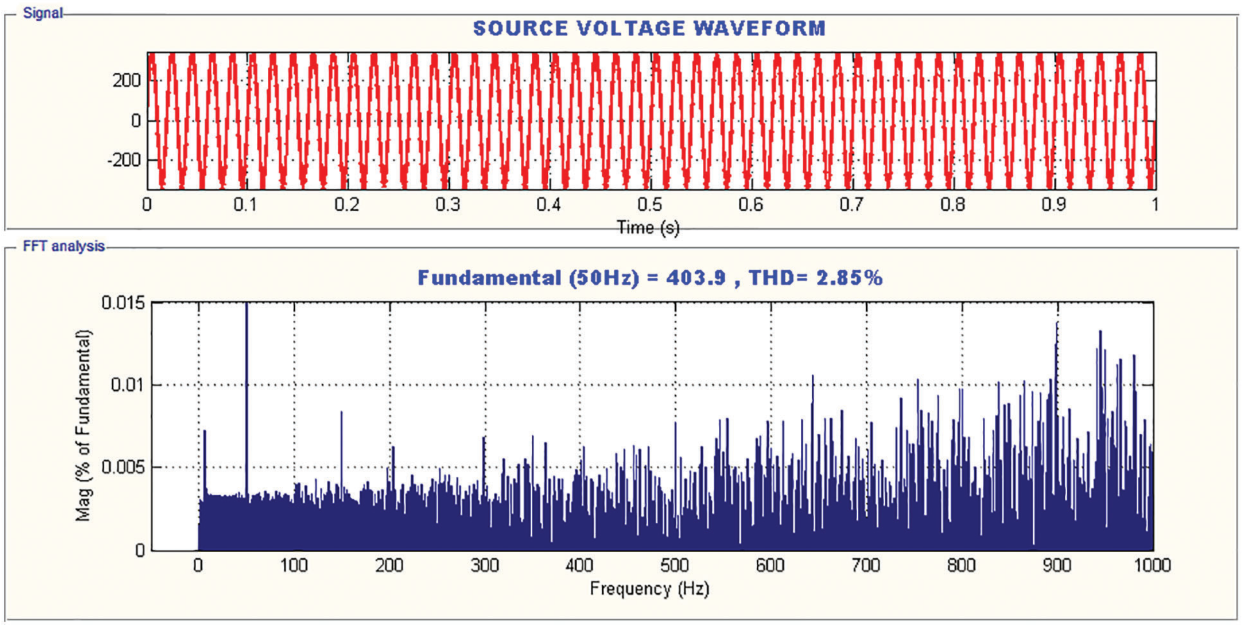

Figure 17: Source voltage THD waveform using PI controller

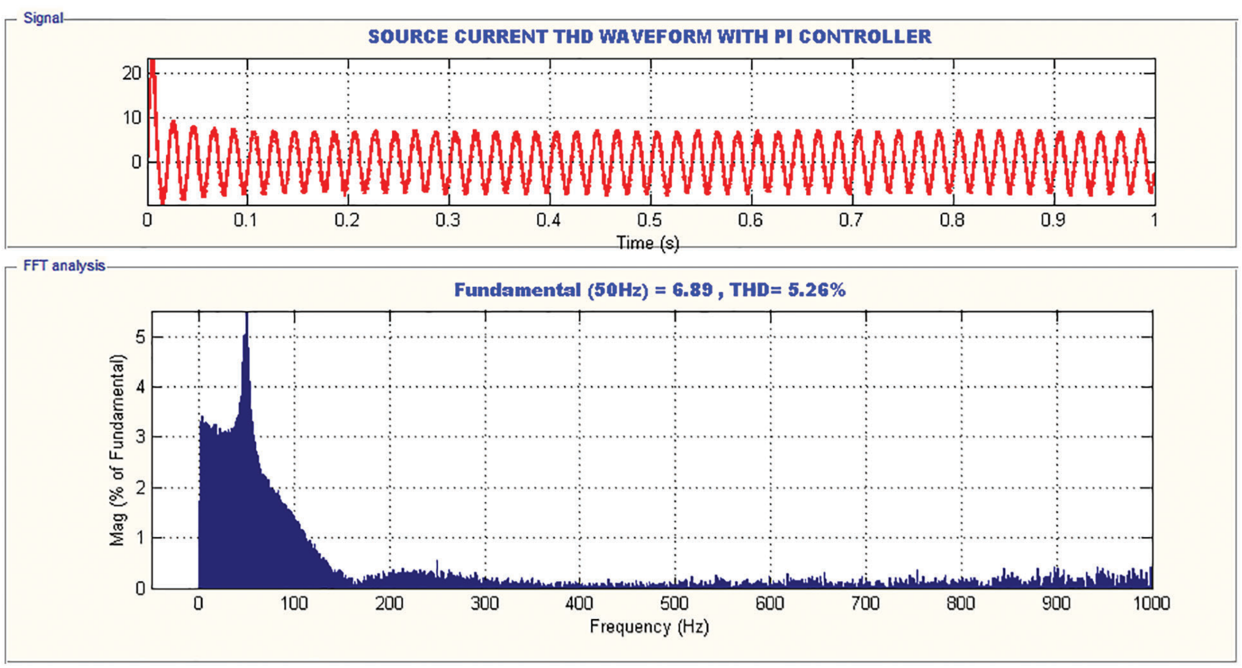

Figure 18: Source current THD waveform using PI controller

The Source voltage and current THD waveform using FLC is depicted in Figs. 19 and 20. When comparing to proportional integral controller, total harmonic distortion is very low in FLC. This is achieved by means of Mamdani method in fuzzy logic controller.

The waveform of PCC potential and current is depicted in Fig. 21. The source voltage is fed to non-linear load, it produces harmonics. By using DSTATCOM it becomes sinusoidal. This produces equivalent opposite harmonics. After the working of DSTATCOM, the harmonics present in DSTATCOM opposes the equivalent opposite harmonics.

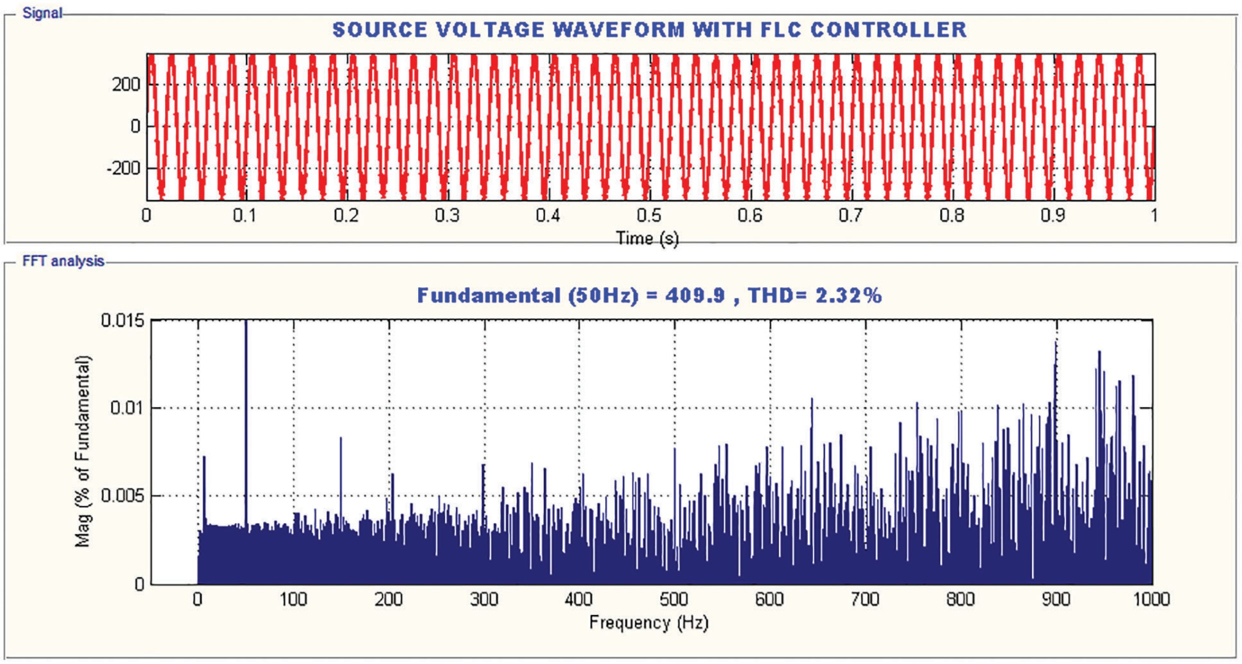

Figure 19: Source voltage THD waveform using Fuzzy logic controller

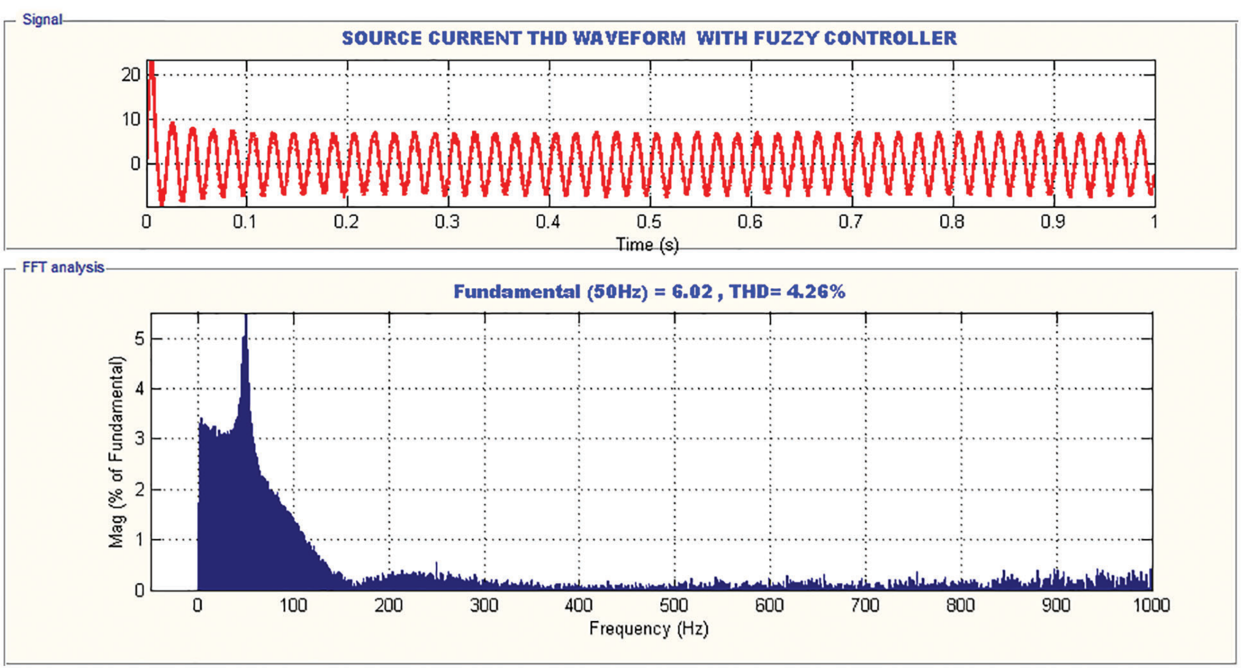

Figure 20: Source current THD waveform using Fuzzy logic controller

The waveform of source voltage and current after compensation is depicted in Fig. 22. The current waveform is injected in the PCC. Due to non-linear load this voltage is affected by means of harmonics. So this harmonics is minimized by means of DSTATCOM. The harmonics present in the source current are reduced by means of reference current theory based hysteresis current controller.

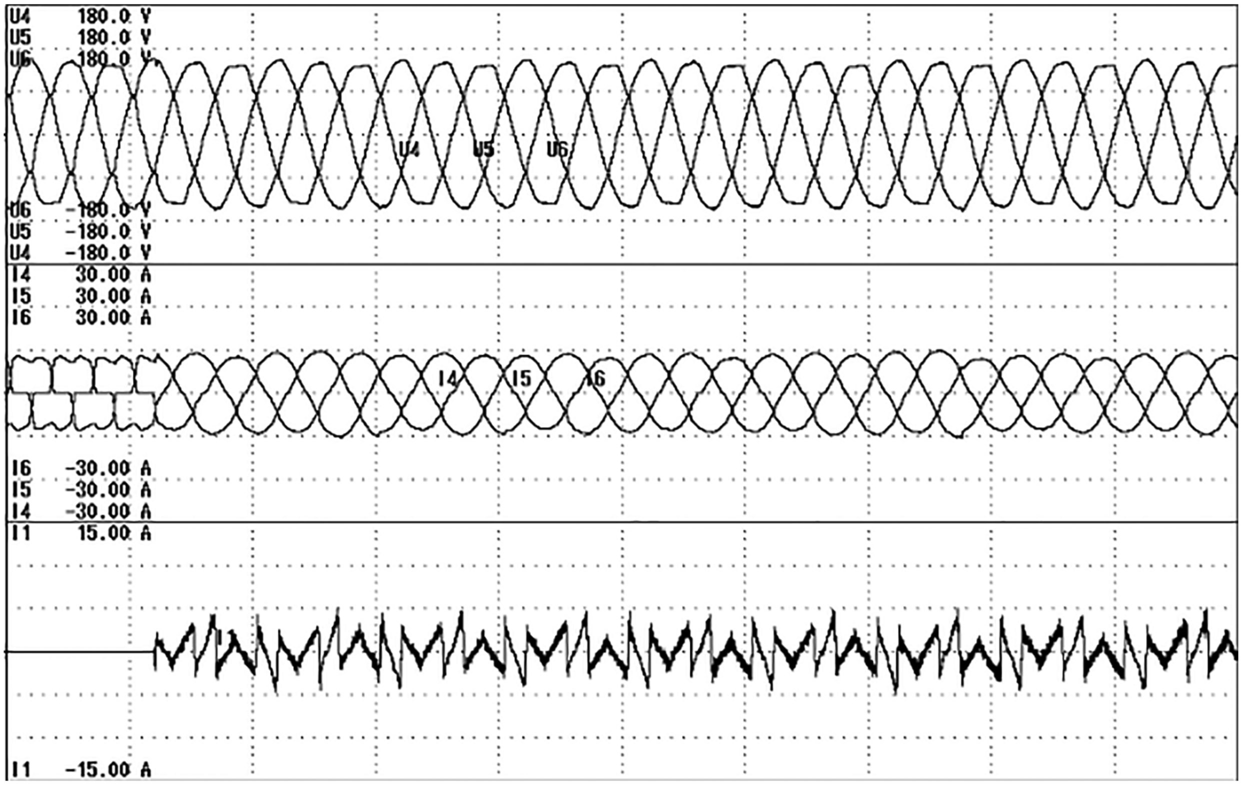

Figure 21: PCC voltage and current waveform

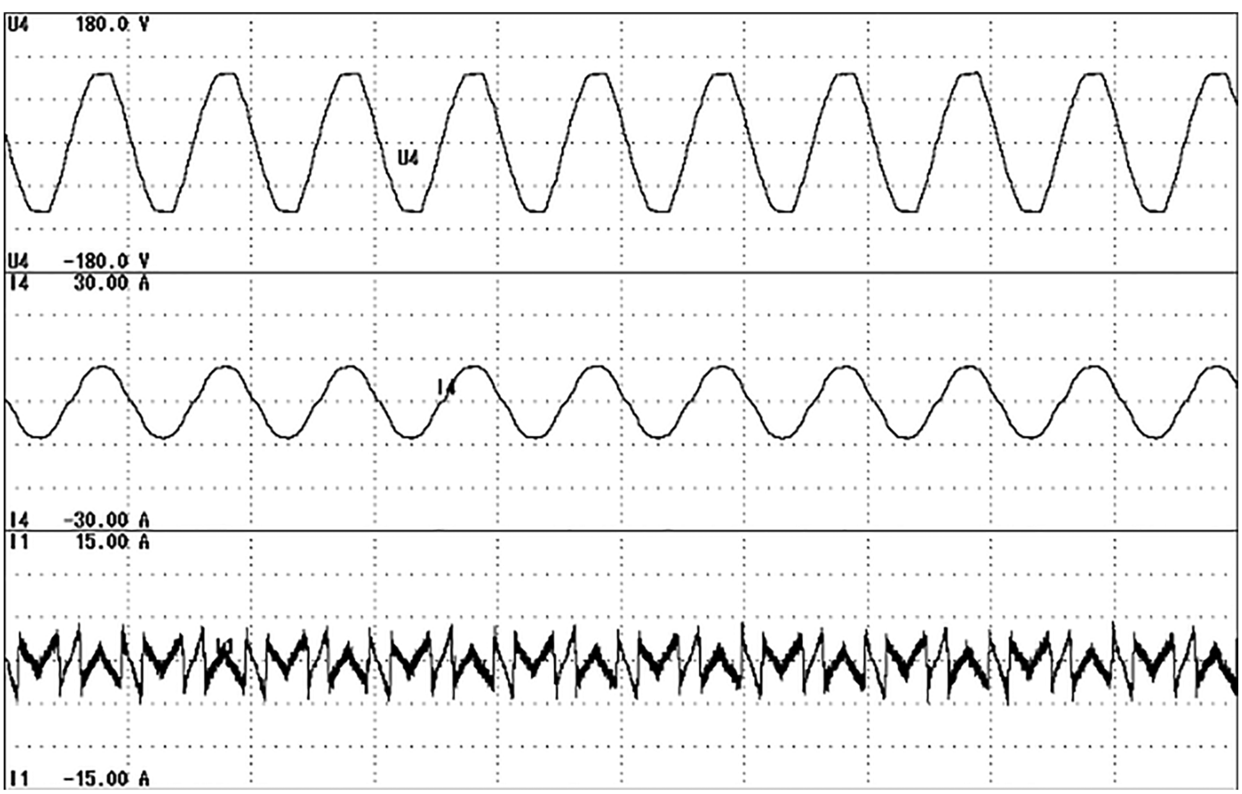

Figure 22: Source voltage and current waveform

The Fig. 23 shows THD current waveform. By using PI controller harmonics is high and maximum peak overshoot. To overcome this drawback, FLC is employed this reduces harmonics. The THD is only 4%.

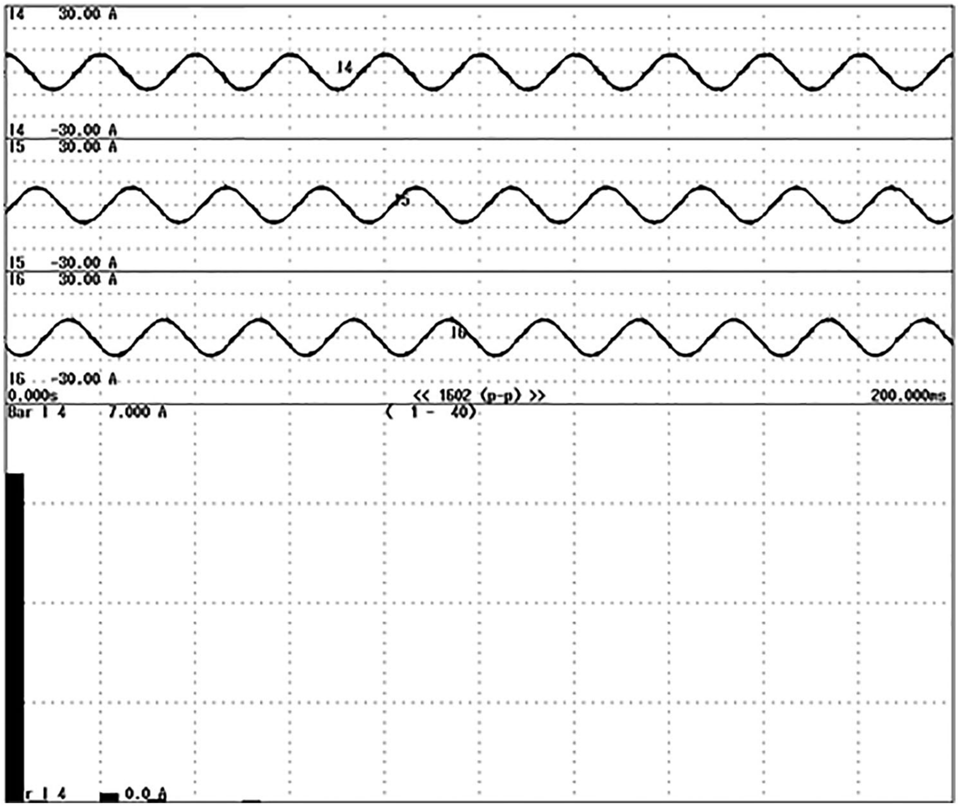

Figure 23: Current THD waveform

The Fig. 24 shows the waveform of multilevel level inverter output voltage waveform. Multilevel inverter output converts DC to AC, through inductor opposite harmonics are injected to PCC reduces harmonics and reactive power.

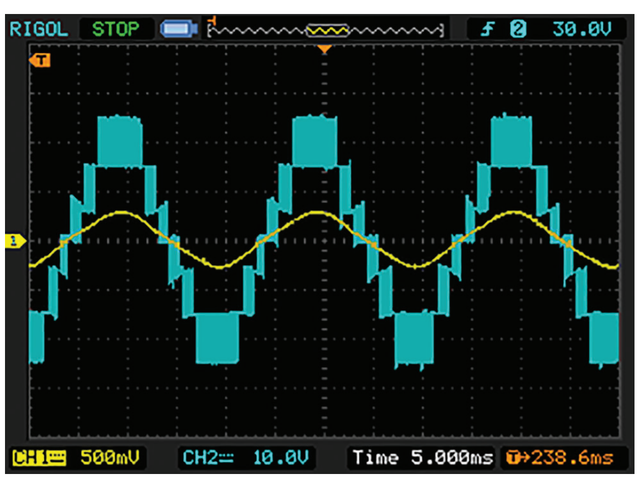

Figure 24: MLI output voltage waveform

8 Conclusion

The shunt connected DSTATCOM based seven level cascaded H-bridge inverter is developed. The behavior of seven level cascaded H-bridge inverter using DSTATCOM is estimated for reactive power compensation, harmonic compensation under non-linear load. Distribution Static Compensator (DSTATCOM) aid to enhance power factor as well as it removes total harmonic distortion which is supplying from non-linear load. D–Q reference theory is employed to generate reference current for compensation of harmonics and reactive power, additionally Probabilistic Neural Network (PNN) classifier is used which easily separates exact harmonics. Conventionally proportional integral controller is employed to keeps DC-link capacitor potential, the drawbacks in PI controller is it increases steady state time and maximum peak overshoot. To overcome this drawback fuzzy logic controller is employed to maintain DC-link capacitor potential. Multilevel inverter converts DC to AC, through inductor opposite harmonics are injected to PCC and therefore in source current harmonics decreases, indirectly real power increases and reactive power decreases.

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