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Improved Interleaved Single-Ended Primary Inductor-Converter for Single-Phase Grid-Connected System

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Abstract: The generation of electricity based on renewable energy sources, particularly Photovoltaic (PV) system has been greatly increased and it is simply instigated for both domestic and commercial uses. The power generated from the PV system is erratic and hence there is a need for an efficient converter to perform the extraction of maximum power. An improved interleaved Single-ended Primary Inductor-Converter (SEPIC) converter is employed in proposed work to extricate most of power from renewable source. This proposed converter minimizes ripples, reduces electromagnetic interference due to filter elements and the continuous input current improves the power output of PV panel. A Crow Search Algorithm (CSA) based Proportional Integral (PI) controller is utilized for controlling the converter switches effectively by optimizing the parameters of PI controller. The optimized PI controller reduces ripples present in Direct Current (DC) voltage, maintains constant voltage at proposed converter output and reduces overshoots with minimum settling and rise time. This voltage is given to single phase grid via 1Φ Voltage Source Inverter (VSI). The command pulses of 1Φ VSI are produced by simple PI controller. The response of the proposed converter is thus improved with less input current. After implementing CSA based PI the efficiency of proposed converter obtained is 96% and the Total Harmonic Distortion (THD) is found to be 2.4%. The dynamics and closed loop operation is designed and modeled using MATLAB Simulink tool and its behavior is performed.

Keywords: Improved interleaved DC-DC SEPIC converter; crow search algorithm; PI controller; voltage source inverter; PV array; single phase grid

ABBREVIATIONS

PV	Photovoltaic
CSA	Crow Search Algorithm
SEPIC	Single-ended Primary Inductor-Converter
PI	Proportional Integral
DC	Direct Current
VSI	Voltage Source Inverter
THD	Total Harmonic Distortion

MIC	Module-integrated converters
L-C	inductor-capacitor
VSS-LMS	Variable Step Size-Least Mean Square
PCC	Point of Common Coupling
SPV	Solar PV
UPF	Unified Power Flow
CSI	Current Source Inverter
GSA	Gravitational Search Algorithm
FLC	Fuzzy Logic Control
MPPT	Maximum power point tracking
GWO	Grey Wolf Optimization
GD	Gradient Descent
PSO	Particle Swarm Optimization
AC	Alternating Current
SC	Short Circuit
OC	Open Circuit
PLL	Phase Locked Loop
PD	Phase Detector
LP	Loop filter
VCO	Voltage Controlled Oscillator
LPF	Low Pass Filter
CCM	Continuous Conduction Mode

SYMBOLS

V_{ref}	Reference voltage
V_{act}	Actual voltage
I_{ph}	Photocurrent
V_{OC}	Open circuit voltage
R_s	Series resistance
I_{sc}	Short circuit current
R_{sh}	Shunt resistance
K_V	Voltage per temperature coefficient
T	Temperature
q	Electron charge
K_i	Current per temperature coefficient
$V_{in},\ V_{out}$	Input and output voltage
$\Delta i_{L_1},\ \Delta i_{L_2}$	Peak to peak ripples in inductor currents
I_{in}, I_{out}	Input and output currents
$L_1,\ L_2$	Input inductors of the converter
$L_3,\ L_4$	Output inductors of the converter
$C_1,\ C_2$	Middle capacitors of the converter
Δv_{out}	Peak to peak ripple of coupling capacitor voltage
C_{out}	Output capacitor
K_p & K_i	Proportional gain & Integral gain
V_m	Amplitude
θ	Angle
ω	Frequency
Φ	Phase angle of input signal
ζ	Damping ratio

1 Introduction

The world's rising demand for electricity has improved the productivity and widespread use of renewable energy. Among most significant renewable energy sources utilized for power generation, solar PV array has attracted most of the researchers [1]. The PV system typically consists of PV panels that are linked in a combination of series-parallel to meet centralized power inverter's high input voltage specifications for grid connections. The PV array based Sub module-integrated converters (subMICs) have the ability of increasing the production of PV energy by eliminating losses in power that arise owing to intra panel mismatch. The double-frequency ripple occurs because of 1Φ grid and gets reflected as fluctuations of solar output as well as current in DC-link voltage [2]. In a PV array, mismatched power losses are minimized by using distributed power electronics at the Sub module stage [3]. The traditional compensation scheme based on discrete inductor-capacitor (L-C) banks has harmful issues on feeder voltage waveforms. To overcome these issues, a feasible scheme based on distributed generation system is proposed for improving the capability of solar array reactive power by removing switching transients [4]. A multifunctional linear quadratic regulator based single-stage residential photovoltaic power supply is introduced to compensate harmonic currents produced by distorted input voltage [5]. To improve the behaviour of single level PV tied grid scheme, a modified Variable Step Size-Least Mean Square (VSS-LMS) based adaptive control is presented for attaining required potential at Point of Common Coupling (PCC) and removes harmonics when transferring all power and loads to the grid [6].

A 1Φ single-stage solar PV (SPV) interfaced multifunctional grid scheme is proposed. Since it has maximum power point tracking (MPPT), the proposed SPV scheme removes harmonics, compensates reactive power and at Unified Power Flow (UPF) it feeds SPV energy into grid [7]. A 1Φ single-stage Current Source Inverter (CSI) dependent solar PV tied grid system is discussed. This method uses transformer-less single-level conversion to track MPPT as well as interfacing PV array to grid [8]. The modular grid integrated 1Φ scheme implemented on module-integrated converters (MIC) in which the current source is connected in series manner is presented to enhance reliability & redundancy of solar distributed generator [9]. The non-isolated high step-up DC-DC converter with double linked inductance appropriate for grid linked solar array is approached. By using series connected dual coupled inductors at output side, this scheme attains high voltage gain [10]. In grid connected network, high voltage boosting leads to decrease in efficiency. To overcome this problem, a new higher potential gain, higher efficiency DC-DC converter implemented on coupled inductance is proposed [11]. An integrated DC-link voltage and MPPT control is proposed by utilizing a single stage DC-DC converter. This approach provides reactive power compensation with reduced harmonics and supplies the power to grid [12]. A soft-switched DC-DC converter is proposed with the utilization of additional simple resonant cell for improving the energy conversion efficiency. It reduces the conduction losses and switching losses thereby minimizing the energy loss of the system [13].

Design of sliding mode controller for photo voltaic MPPT is proposed. This is fed to SEPIC converter and it is applied to a broad variety of PV fed converters [14]. A PV system interfaced with SEPIC converter is proposed to reduce the oscillations occurring in the maximum power point. It provides positive load voltage with non-pulsating nature of load current [15]. Depending on the availability of solar energy, both synchronous SEPIC as well as Zeta converter via MPPT photo voltaic array overcome the problem of rise in power demand [16]. The synchronous Cuk converter based solar array is presented to minimize losses due to conduction and switching [17]. An improved DC-DC converter dependent on the integration of Cuk as well as single ended primary inductor converter is introduced for SPV applications. This converter utilizes only 1 switch but offers double outcome of bipolar DC bus [18]. An adaptive controller containing PI and Fuzzy optimizes the system adaptable. A new optimized proportional integral derivative controller for SEPIC MPPT based converter is proposed. In terms of device response as well

as input exploitation, the proposed Gradient Descent (GD) technique provides better performance than traditional GD [19,20].

A Fuzzy Logic Control (FLC) based SEPIC for MPPT is proposed. With reduced voltage stress, this SEPIC has high stepped potential design. The Zeta converter's output current is continuous with lesser output ripple compared to SEPIC and Cuk converters [21]. Using Grey Wolf Optimization (GWO), a MPPT design for solar array is proposed to overcome the drawback of lesser tracking efficiency and steady-state oscillations [22]. A novel Cuk–SEPIC converter dependent PV with hybrid GSA and PSO using MPPT minimizes ripples present in input current that aid maximum utilization of PV system [23]. The algorithm of perturb and observe suffers from lack of tracking direction issue and likely fails during huge insulation transformation condition. Through enhancement in perturb and observe algorithm, efforts were made to resolve these problems [24]. The latest optimized algorithms are incapable to resolve whole optimization difficulties. The combined optimization technique which improves the power tracking performance due to its simple implementation is crow search optimization, a finest algorithm which is used in hybrid combinations [25].

An improved interleaved DC-DC SEPIC converter is employed in proposed work. This converter boosts up the PV panel DC voltage. Conventionally PI controller is utilized for controlling DC link voltage. The parameters of PI are tuned by CSA. By optimizing PI controller with CSA, the ripples are reduced and constant voltage is maintained at proposed converter output with reduced settling time. This voltage is fed to 1Φ VSI that converts DC to Alternating Current (AC). A constant AC output voltage obtained is synchronized perfectly with the grid voltage using closed loop PI controller.

2 Proposed System

The proposed system's schematic block representation presented in Fig. 1. It is composed of PV panel and is coupled with an improved interleaved DC-DC SEPIC converter that consists of four inductances and capacitances, two switches and diodes. As this converter circuit is having four inductances and capacitances, it is known as fourth order filter. At the input side it consists of PV panel with a voltage of 80 V DC. This PV panel depends upon two inputs i.e., temperature and intensity. If the temperature and intensity is varied, PV panel voltage also changes. Therefore, PV panel voltage is not maintained at constant value and ripples occur. These issues are overcome by using an improved interleaved DC-DC SEPIC converter.

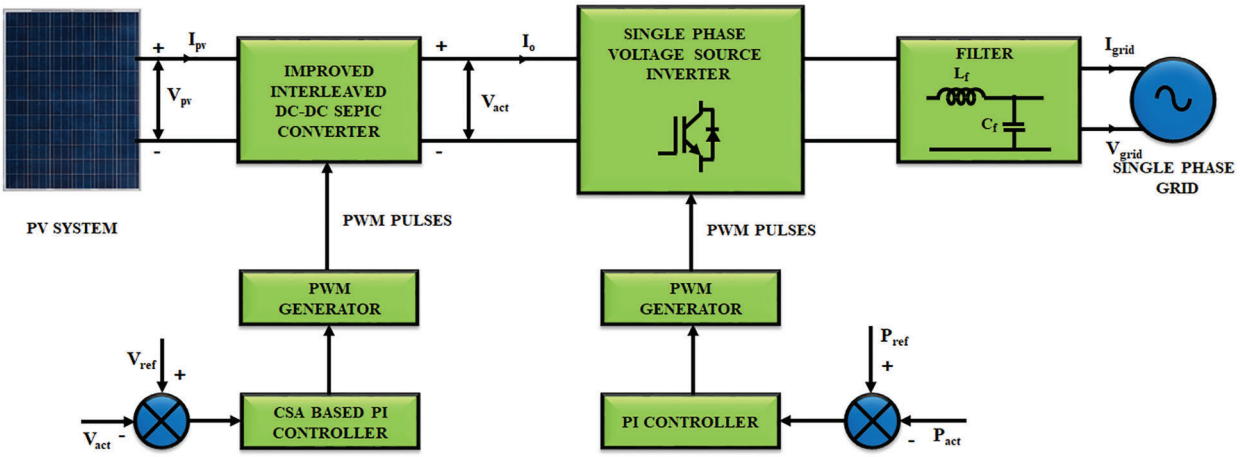


Figure 1: Proposed block diagram

The input voltage of 80 V DC is converted to 270 V DC by means of proposed converter. Normally, output in SEPIC attains 80% duty cycle but in proposed converter, it attains duty cycle of $52-53\%$. The ripples present in PV panel voltage is easily removed by proposed converter. The input current is continuous due to the presence of inductance at input of proposed converter. It's voltage at the output is maintained by PI controller whose parameters are varied by crow search algorithm indicating the novelty of the approach. In this algorithm, reference voltage V_{ref} is set at initially and then actual voltage V_{act} is measured. On comparing both V_{ref} & V_{act} values, error is generated and this error is given to PI. The parameters of PI are tuned by crow search algorithm and outcome of proportional integral controller is further compared with high frequency carrier signal. The comparator output is given to PWM generator for the generation of pulses to be applied to the improved interleaved DC-DC SEPIC converter. Now converter's outcome voltage of 270 V DC is fed to 1Φ VSI, which converts DC into AC so as to feed it to grid. The entire process is significantly illustrated in Fig. 2 in an efficient manner.

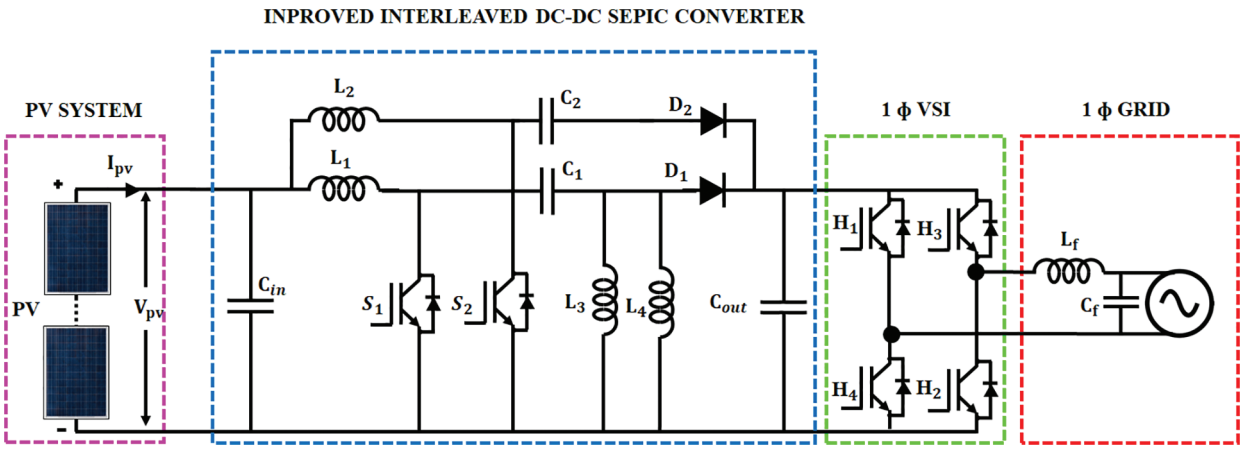


Figure 2: Schematic representation of PV fed improved interleaved DC-DC SEPIC converter

3 Modeling of Proposed System

3.1 Modeling of PV Panel

A solar cell is a tool used for conversion of photon energy into pollution-free electricity. The modules connected into series and parallel arrangements are responsible for producing clean and green electricity in order to create PV arrays. As a part of an electrical circuit, a single solar cell is depicted. It involves a p–n junction known as diode, a photocurrent generator illustrating the generation of light current and two resistors. One is arranged in series combination and another one in parallel defining the losses of Joule effect and recombination. This combination is then referred as a single model of PV cell diodes. The equivalent circuit of 1 diode model of photo voltaic cell is depicted in Fig. 3.

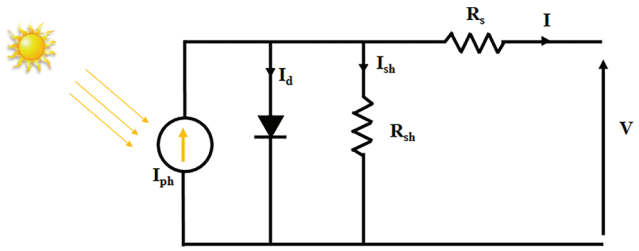


Figure 3: Equivalent circuit of PV panel

The model of PV panel is expressed mathematically as,

$$I = I_{ph} - I_s\left(exp\frac{q(V + R_sI)}{aKTN_s} - 1\right) - \frac{(V + IR_s)}{R_{sh}} \tag{1}$$

$$I_{ph} = (I_{sc} + K_i(T - 298.15))\frac{G}{1000} \tag{2}$$

$$I_s = \frac{I_{sc} + K_i(T - 298.15)}{exp(q((V_{OC} + K_V(T - 298.15))/aKTN_s)) - 1} \tag{3}$$

Thus the physical performance of solar panel depends on resistance connected in shunt and series fashion, solar irradiation and temperature.

3.2 Improved Interleaved DC-DC SEPIC Converter

In solar PV application, converters that are commonly used have faced serious issues on high input current ripples. This issue is overcome by instigating improved interleaved SEPIC converter. An interleaved DC-DC SEPIC converter contains multi-converter phase shifting control signal that works at equal switching frequencies. As a DC–DC converter, it produces extra power, minimizes harmonic distortion, and reduces electromagnetic interference and the schematic representation is mentioned in Fig. 4.

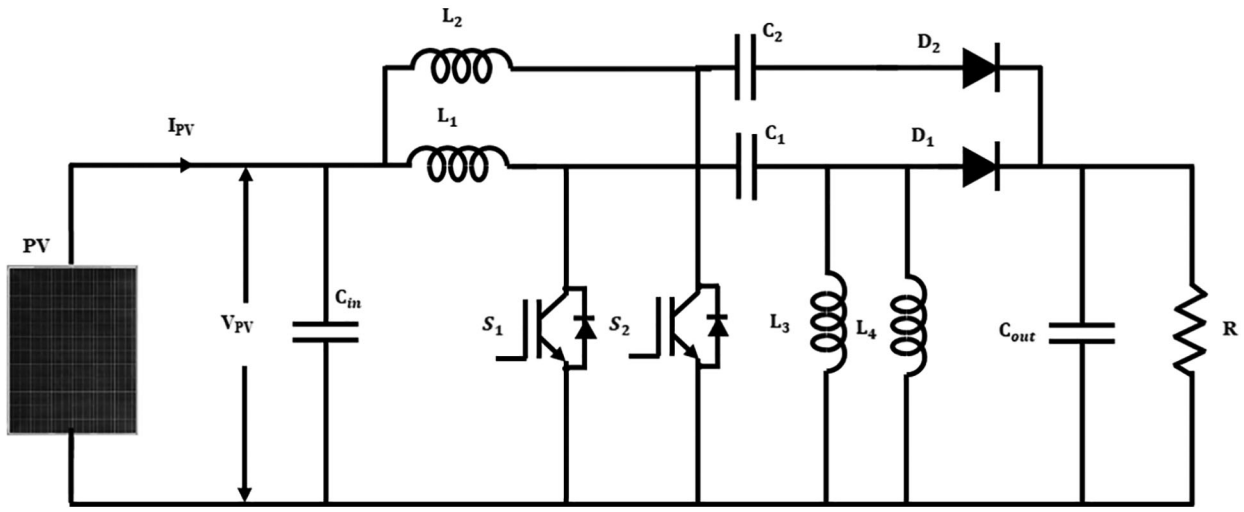


Figure 4: Circuit diagram of improved interleaved DC-DC SEPIC converter

The proposed converter delivers an outstanding conversion of buck-boost with non-inverted output potential which is compared to other interleaving DC–DC converters and achieves greater energy efficiency with minimum elements. The output voltage (V_{out}), inductances and capacitances' equations for designed converter are expressed in steady state as given below,

$$\frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{d}{d-1} \tag{4}$$

$$L_1 = L_2 = \frac{(1-d)V_{out}}{\Delta i_{L_1} f_{sw}} = \frac{(1-d)V_{out}}{\Delta i_{L_2} f_{sw}} \tag{5}$$

$$L_3 = L_4 = \frac{L_1}{2} = \frac{L_2}{2} \tag{6}$$

$$C_1 = C_2 = \frac{dI_{out}}{\Delta v_{out} f_{sw}} \tag{7}$$

$$C_{out} = \frac{dP_{out}}{\Delta v_{ripple} V_{out} f_{sw}} \tag{8}$$

Thus the interleaved SEPIC converter performs efficient boosting of input DC voltage with the generation of reduced electromagnetic interference and ripples.

3.3 CSA Based PI Controller for Proposed Converter

The PI controller parameters K_p & K_i are used to control DC link voltage of PV interface system. These parameters are tuned using CSA optimization. Between reference voltage and actual voltage there will be an error and the objective function is used to minimize the error. By optimizing PI controller parameters using CSA, the settling time, ripples and rise time are reduced.

Crows are regarded as clever birds having brilliant brain. The unfavorable condition is simply predicted by crows as they are having great capacity of face recognition. It will search for its food in an optimal manner by interacting with their families.

For instigating CSA, the parameters are regarded as follows.

No. of crows allocated as flock size is denoted as N, location of crow i at period of time i.e., iteration k in search room, Maximum iteration is denoted as M. Every crow has its own memory to remember location of concealed area. At iteration k, location of concealed crow i is named as at $m^{i,k}$ which is the finest location that crow i has attained.

Consider, crow j monitor hiding area i.e., $m^{i,k}$ at iteration M. On this instant crow i choose to watch crow j to reach concealed area of crow j. In these procedures, there are two conditions as follows,

Condition 1: Crow j is unaware about the watching of crow i. Hence, concealed area of crow j is monitored by crow i. At this instant, new location of crow i attained is given below,

$$x^{i,\,k+1} = x^{i,\,k} + (r_i \times f^{i,\,k}) \times (m^{i,\,k} - x^{i,\,k}) \tag{9}$$

where, r_i denotes random number with a uniform distribution among 0 *to* 1, $f^{i,\,k}$ indicates length of flight crow i at iteration k.

Condition 2: Crow j realizes that it is being watched by crow i . For protecting its cache from pilfered, it starts moving to another location in the search space so as to fool crow i. By combining these two conditions, the equation is expressed as,

$$x^{i,\,k+1} = \begin{cases} x^{i,\,k} + (r_i \times f^{i,\,k}) \times (m^{i,\,k} - x^{i,\,k}) & r_j \geq AP^{i,k} \\ a\ random\ position & otherwise \end{cases} \tag{10}$$

where, r_j denotes random number with a uniform distribution among 0 *to* 1, $AP^{i,k}$ indicates awareness probability of crow j at iteration k.

3.3.1 Crow Search Algorithm Implementation for Optimization

The steps included in the implementation of crow search algorithm are,

Step 1: First initialize the problem and adjust the tuning parameters**.** The values for optimization problem, variables of decision and constraints are required to be defined. The parameters adjusted in CSA are flock size (N), maximum iteration (M), flight length $(f^{i,\,k})$ and awareness probability $(AP^{i,k})$.

Step 2: Initialize the location and memory of crows. In d-dimensional search place N crows are placed randomly as members of flock. Every crow denotes a possible solution of issue and d denotes the number of decision variables.

Step 3: Calculate fitness function for DC link voltage.

Step 4: Update memory using the expression

$$m^{i,\ k+1} = \begin{cases} x^{i,\ k+1} & F(x^{i,\ k+1}) > F(m^{i,k}) \\ m^{i,\ k} & otherwise \end{cases} \tag{11}$$

If the value of fitness function for DC link voltage of new crow location is greater than the value of memorized location, the crow updates its memory with the new location.

Step 5: Crows create novel location in search place as crow i is required to create novel location. This crow chooses a flock crow and pursues it to find location of concealed foods. For all the crows, the procedure is repeated.

Step 6: It tests the feasibility of novel location of every crow. If novel location of crow is viable, crow will update its location, otherwise crow will remain in its current location.

Step 7: Again calculate fitness function for DC link voltage.

Step 8: Until the iteration attains the value of maximum iteration, repeat the steps from 4–7. The finest position of memory in terms of DC link voltage as objective function is determined by controller's optimal gain values.

The obtained values from the CSA optimization indicates efficient tuning of PI controller parameters. This maintains a constant DC link voltage with minimized ripples and settling time. The flowchart representing this process is evidently provided in Fig. 5.

3.4 Grid Synchronization in Single Phase PV System

Fig. 6 shows the control structure of 1Φ grid linked PV panel where grid detection and synchronization plays a major role. If non-linear load is applied at PCC, there is a potential drop at the point, detection and synchronization scheme responds abnormal condition immediately as a protection measure. Therefore, for producing accurate reference signals via potential drop within a given time, it is required to implement a quick and precise synchronization technique.

Normally, synchronization methods are classified in to two types as mathematical analysis method and PLL method. Among these methods, adaptive filtering based phase locked loop method gains more attraction. A fundamental PLL is represented in Fig. 7.

The structure of PLL contains PD, LP and VCO. If first order LPF is utilized, a small signal model of 1Φ PLL becomes a second order scheme that is expressed as,

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_1K_2G_{lf}(s)}{s + K_1K_2G_{lf}(s)} = \frac{K_1K_2K_ps + K_1K_2K_i}{s^2 + K_1K_2K_ps + K_1K_2K_i} \tag{12}$$

where, $\theta_o(s)$, $\theta_i(s)$ denotes output and input phase, K_1, K_2 denotes gains of phase detector and voltage controlled oscillator. Transfer function of Loop factor is expressed as,

$$G_{lf}(s) = K_p + K_i/s \tag{13}$$

where,K_p, K_i denotes proportional and integral gains of loop factor.

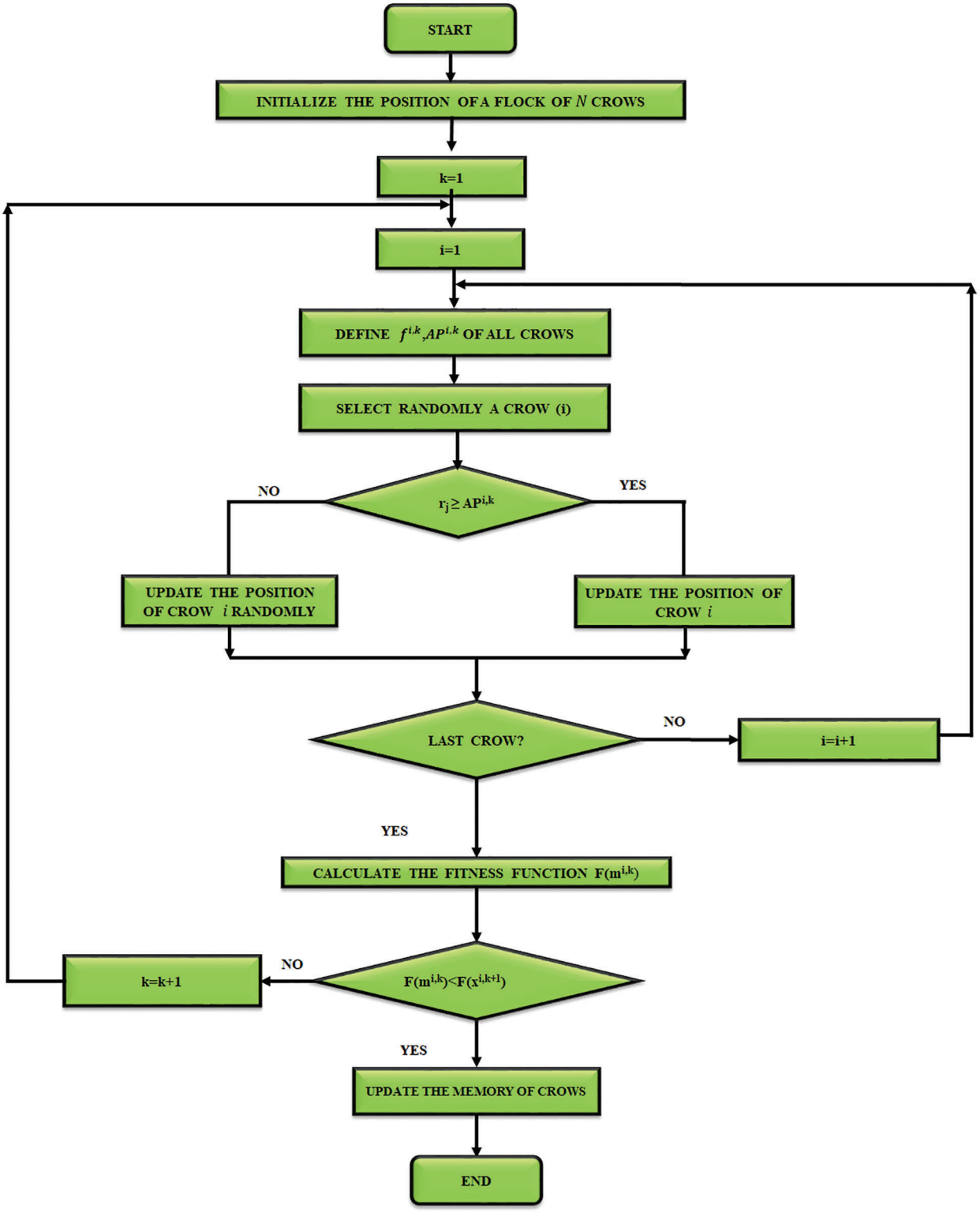


Figure 5: Flow chart of crow search algorithm

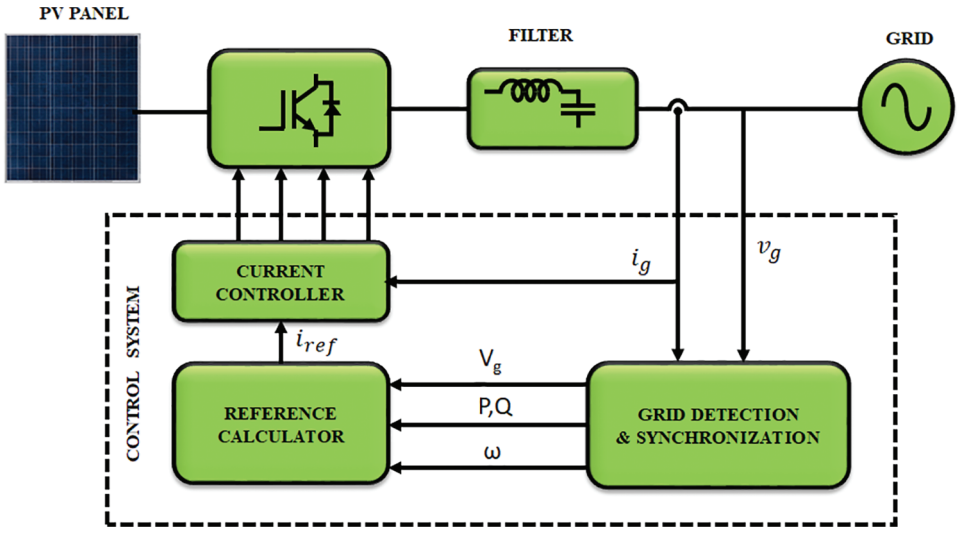


Figure 6: Control structure of 1Φ grid connected PV system

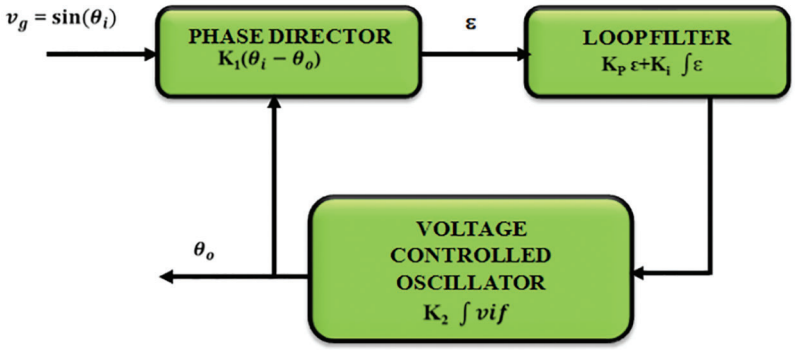


Figure 7: Basic PLL

From Eq. (12), damping ratio and undamped natural frequency are given by,

$$\zeta = \frac{1}{2}\frac{K_p}{\sqrt{K_i}}, \quad \omega_n = \sqrt{K_i} \tag{14}$$

when $K_1 = K_2 = 1$. The settling time is attained as,

$$t_s = \frac{4.6}{\zeta \omega_n} \tag{15}$$

The use of adaptive filter is another option for phase detection that perform self-adjusting of output using an error feedback loop.

3.4.1 T/4 Delay Phase Locked Loop

Considering an ideal sinusoidal signal, $v_i = V_m \sin(\theta) = V_m \sin(\omega t + \Phi)$, Where, V_m denotes amplitude, θ denotes angle, ω denotes frequency and Φ denotes phase angle of input signal. This is chosen as $''\alpha''$ element of $''\alpha\beta''$ scheme and $''\beta''$ element is attained as phase shift of $\frac{\pi}{2} rad$ w.r.t fundamental frequency of input potential. Therefore, park transform i.e., $\alpha\beta \rightarrow dq$ is utilized in this

scheme for detecting phase error that is represented as,

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} cos\hat{\theta} & sin\hat{\theta} \\ -sin\hat{\theta} & cos\hat{\theta} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} V_m \sin(\Delta\theta) \\ -V_m \cos(\Delta\theta) \end{bmatrix} \tag{16}$$

where, $\Delta\theta = \theta - \hat{\theta}$ is phase error detection, $\hat{\theta}$ denotes locked phase angle. Normally, error $\Delta\theta$ is so less in steady state, so linearized equations is written as,

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} \approx \begin{bmatrix} V_m \Delta\theta \\ -V_m \end{bmatrix} \tag{17}$$

Using PI controller v_d is controlled to zero and input signal phase is locked. This type of phase locked loop is known as $T/4$ Delay PLL, where, T denotes input signal fundamental period. The schematic structure of $T/4$ Delay Phase Locked Loop is depicted in Fig. 8.

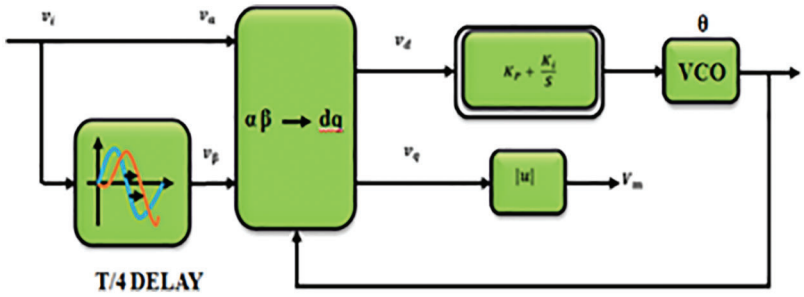


Figure 8: Structure of $T/4$ delay phase locked loop

The $T/4$ Delay phase locked loop is a simplest method which utilizes phase angle extraction in 1Φ applications. On comparing reference signal with carrier signal, it gives PWM pulses. These pulses are given to 1Φ VSI and grid synchronization is carried out.

4 Results and Discussions

The solar array output voltage is fed to an improved interleaved DC-DC SEPIC converter. Due to temperature variation, PV panel output link voltage does not maintain constant value and causes the occurrence of ripples. The CSA based proportional integral controller for proposed converter optimizes PI controller parameters that maintains constant voltage at proposed converter, reduces ripples and settling time. This voltage is given to 1Φ grid through 1Φ VSI that converts DC to AC as it is controlled by PI controller. The design of complete system is validated using MATLAB software and then designed result is checked with hardware implementation.

The solar panel specifications are represented in Tab. 1. The power rating of 1500 W is used. This solar panel voltage is given to converter. The specifications for converter is represented in Tab. 2. The output voltage of converter is optimized by CS-PI controller.

Table 1: Solar panel specifications

Components	Specifications
No. of panel	15
Total no. of series cells	36
Cell area	125 mm × 31.25 mm
Open circuited voltage	21.4 V
Operating current	5.8 A
Short circuited current	6.2 A
Temperature range	−40 to + 85^{0}C
Maximum voltage	1000 V DC
Operating voltage	16.8 V

Table 2: Converter specifications

Components	Symbols	Rating
Input voltage	v_{in}	0 to 120 V
Capacitor	C_1, C_2	25 uF
Inductor	L_1, L_2	5 mH
Input current	i_i	20 A (Max)
Operating frequency	f	10 KHZ
Output load current		10 Amps
Output power	P_0	1500 W
Switches		IRF540
Diodes		MUR1560
Driver circuit		TLP 250
Integral gain	K_i	0.013
Proportional gain	K_p	0.1

4.1 Simulation Results

The simulation results for photo voltaic integrated grid scheme is accomplished in time scale using Simulink that measures performance of converter for a given system. The complete model is obtained from sim-power system tool box. The PV panel voltage and input current waveform is indicated in Figs. 9a and 9b in which the voltage waveform of PV panel observes that voltage changes from 58 V *to* 60 V. This voltage is given to the input of converter.

The output DC voltage waveform using PI controller is represented in Fig. 10a. The output reveals that the voltage does not maintain constancy and so oscillations occur in this waveform. The converter output voltage waveform using CS-PI controller is given in Fig. 10b. It is noted that after 0.15 s, a constant voltage of 270 V DC is maintained.

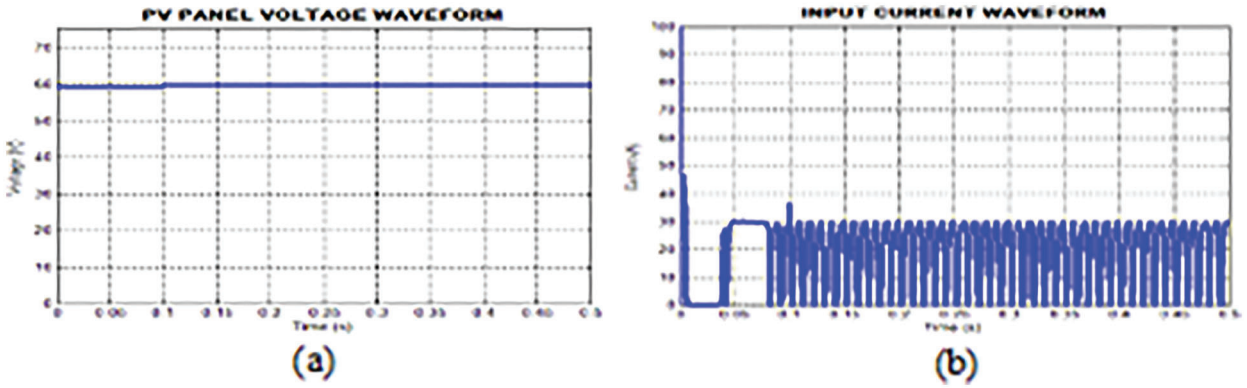


Figure 9: (a) PV panel voltage waveform (b) Input current waveform

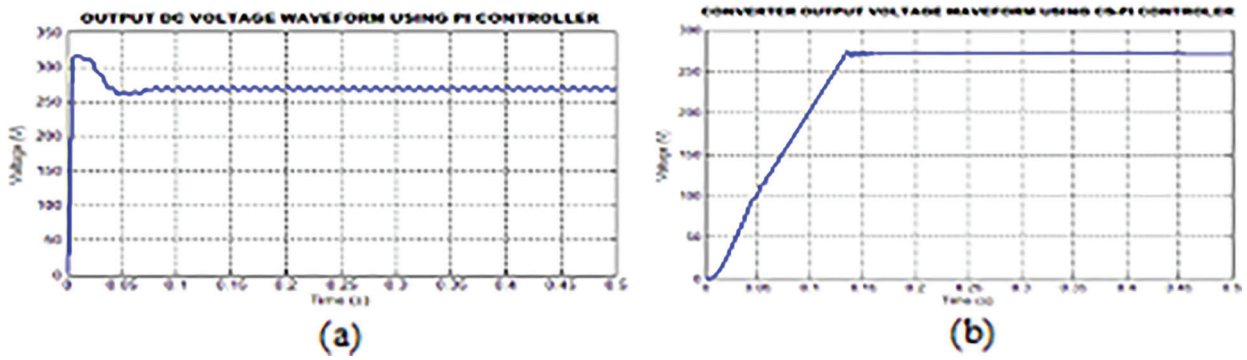


Figure 10: (a) Output waveform of DC voltage adopting PI controller (b) Output voltage waveform of converter adopting CS-PI controller

The output waveform of converter is depicted in Fig. 11. This waveform shows the output current from converter.

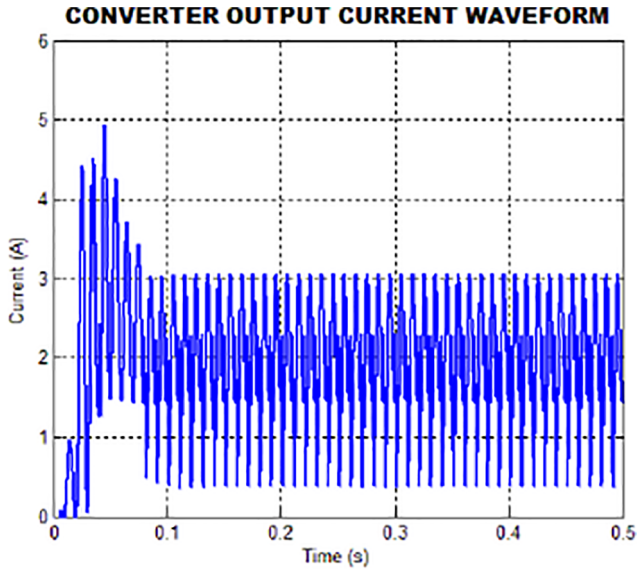


Figure 11: Converter output current waveform

The PWM pulses to the converter switches S_1 and S_2 are depicted in Figs. 12a and 12b. The carrier signal given to PWM generator generates pulses. These pulses operate the switches S_1 and S_2 which is shown in both waveforms.

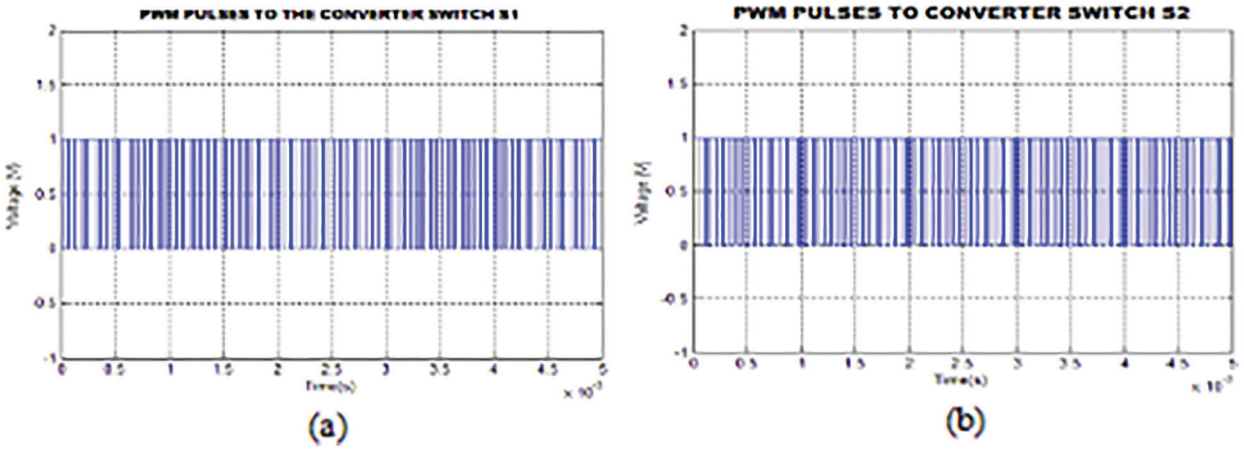


Figure 12: (a) & (b) PWM pulses to the converter switches S_1 and S_2

The waveforms for grid voltage and current are shown in Figs. 13a and 13b. Here, the grid voltage and current are maintained sinusoidal. The harmonics present in inverter current is similar & opposite of load current. The sinusoidal nature of grid current waveform is retained at fundamental frequency with non-linear load.

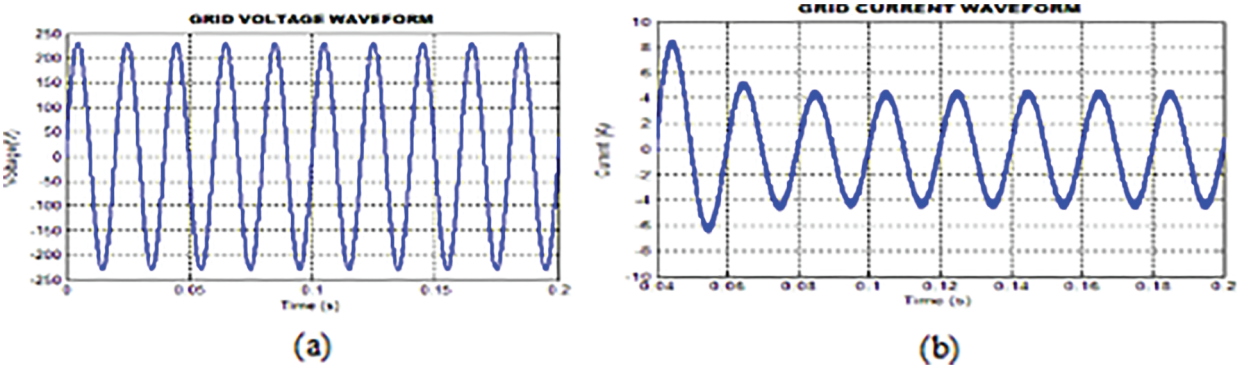


Figure 13: (a) & (b) Grid voltage and current waveform

The real and reactive power waveform is shown in Figs. 14a and 14b. It is noted that the real power decreases and then it attains at maximum power of 1500 W. After the time 0.04 s it decreases and maintains constant power. From the reactive power waveform it is noted that initially it increases and then decreases. After time 0.08 s, it maintains constant value.

The grid current THD with PI and CS-PI is denoted in Figs. 15a and 15b. The behavior of PI and CS-PI controller is measured by evaluating the grid current THD using power analyzer. The grid current THD for conventional PI controller is 4.3% and Grid current THD for CS-PI controller is 1.6%.

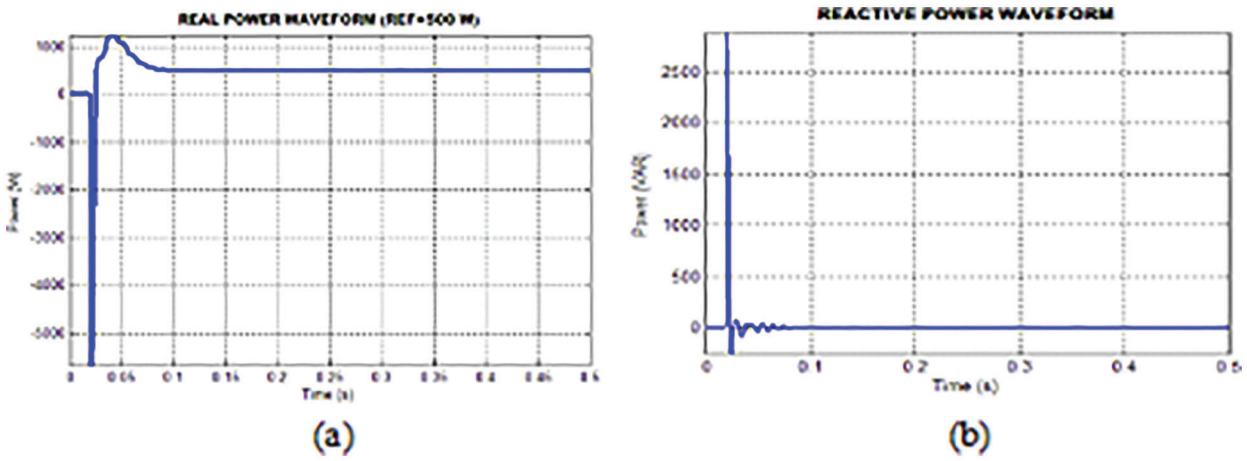


Figure 14: (a) & (b) Real and reactive power waveform

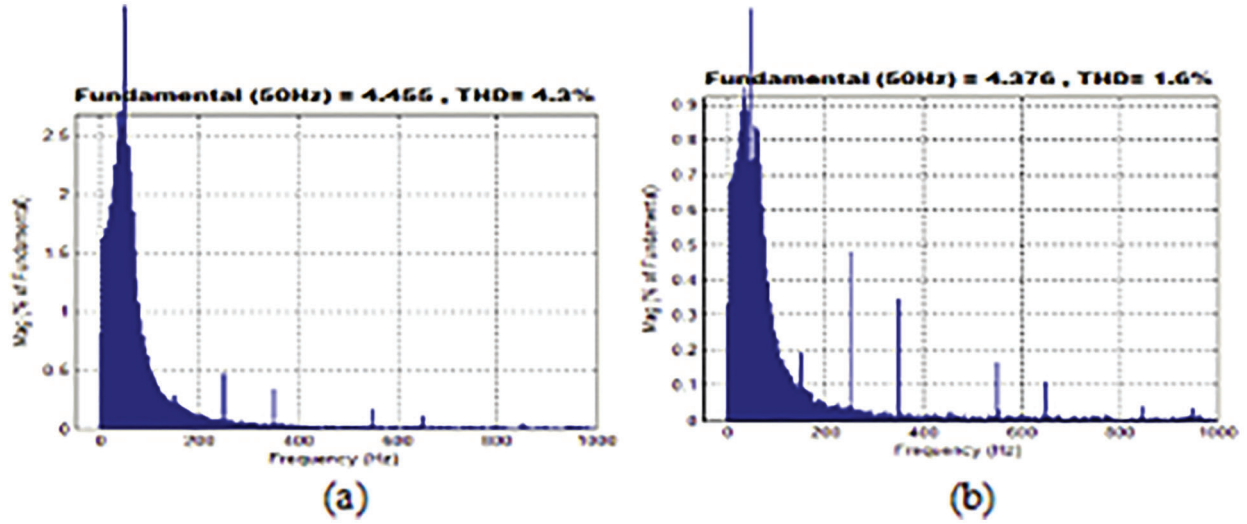


Figure 15: (a) & (b) Grid current THD with PI and CS-PI controller

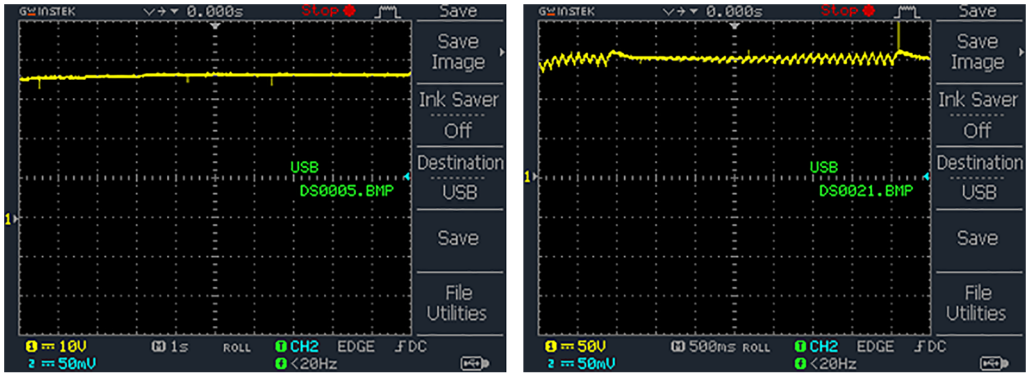
4.2 Results for Hardware Implementation

The DSPIC30F2010 is cost effective since 8 bit microcontroller is used to develop proposed converter system prototype. The DC link voltage is used by the controller which is linked with DC-DC converter as feedback signal. This maintains converter output as steady state. The potential divider as well as Hall Effect sensor are used to measure real power at grid. The signals are performed by signal conditioners and then fed to microcontroller's input point. Using inbuilt Analog to Digital Converter (ADC) unit, the signals are digitized.

The input DC voltage and current waveforms are given in Fig. 16. The PV panel output voltage & current waveform is shown which reveals that the variations occurring in voltage and current is due to temperature changes on PV array. This is given to input of converter.

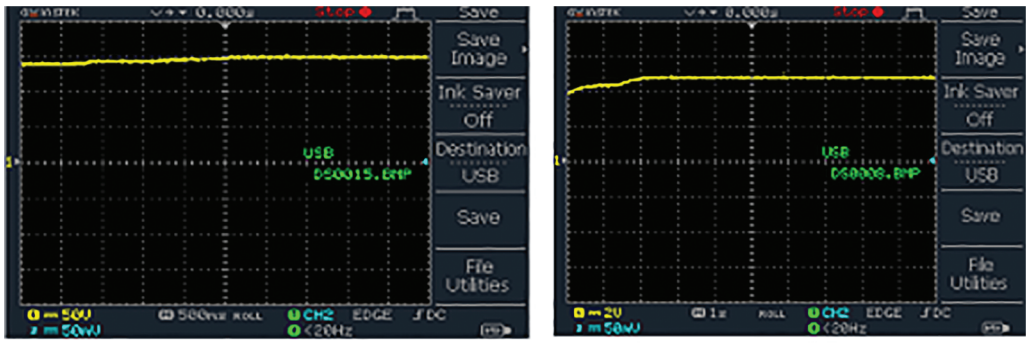
The converter's output voltage waveform for CS-PI controller is depicted in Fig. 17. When comparing this waveform with conventional PI controller, the proposed converter reduces ripples, reduces maximum

peak overshoot, decreases settling time and maintains constant voltage of 270 V DC. The converter output DC current waveform is depicted in Fig. 18. This waveform shows the output current from converter.



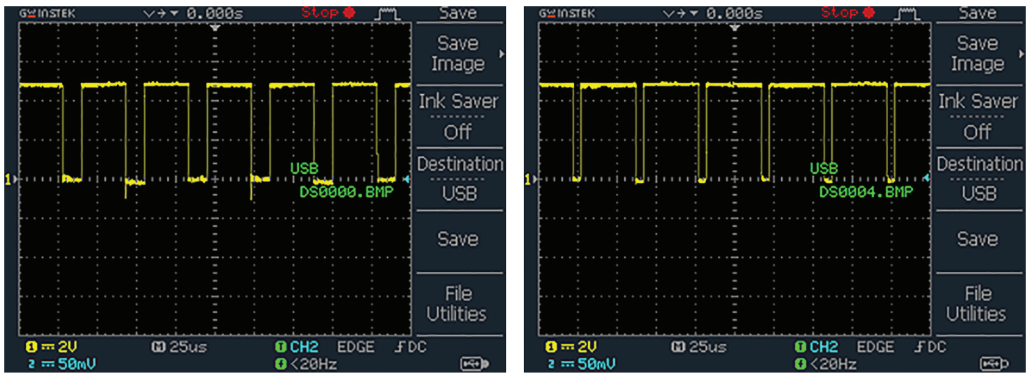
(a) (b)

Figure 16: (a) & (b) Input DC voltage and current waveform



(a) (b)

Figure 17: (a) Converter output voltage waveform for CS-PI controller (b) Output DC current waveform



(a) (b)

Figure 18: (a) & (b) Waveform for PWM pulses S_1 and S_2

The PWM pulses to the converter switches S_1 and S_2 are depicted in Figs. 18a and 18b. The carrier signal given to PWM generator generates pulses. These pulses operate the switches S_1 and S_2 that are shown in both waveforms.

The grid voltage and current waveforms are denoted in Fig. 19. The output of PI controller is combined with sine wave reference extracted from power grid and is given to reference power signal. The output current at inverter is chosen as reference from grid which precisely synchronizes with grid voltage.

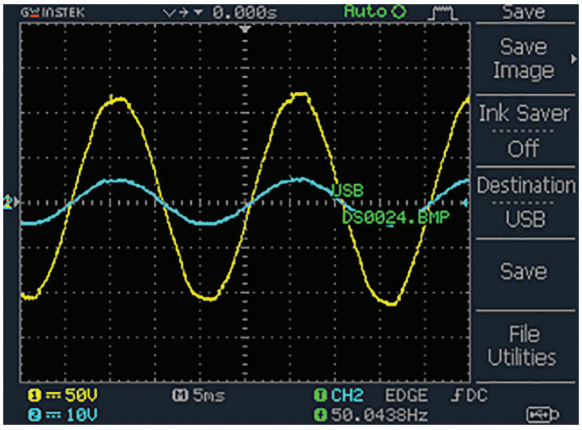


Figure 19: Grid voltage and current waveform

The comparison of efficiency is depicted in Fig. 20. The efficiency of improved SEPIC converter is compared with SEPIC and Boost. From this chart it shows that efficiency of improved SEPIC converter is 96%. It also shows that improved SEPIC converter's performance is better than SEPIC and Boost converter.

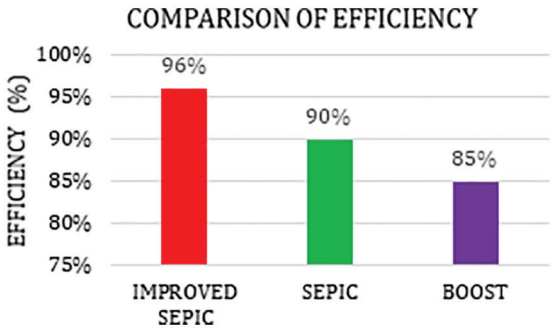


Figure 20: Comparison of efficiency

The comparison of gain is depicted in Fig. 21. The improved SEPIC converter's gain is compared with SEPIC and Boost. From this chart it shows that the improved SEPIC converter's gain is 1:12. It also shows that improved SEPIC converter's performance is better than SEPIC and Boost converter.

The THD comparison is illustrated in Fig. 22. The THD for CS-PI is compared with Fuzzy and PI. From this chart it shows that THD for CS-PI is 2.4%. It also shows that THD for CS-PI performance is better than Fuzzy and PI.

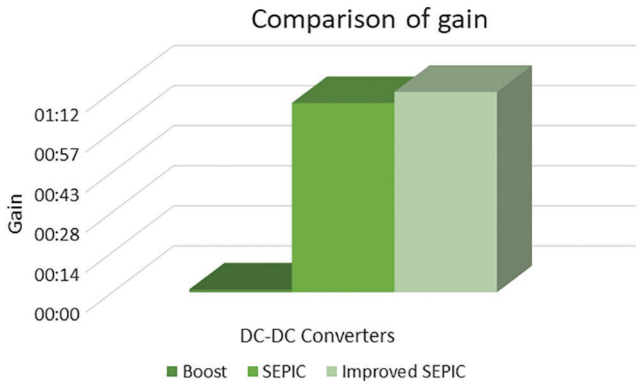


Figure 21: Comparison of gain

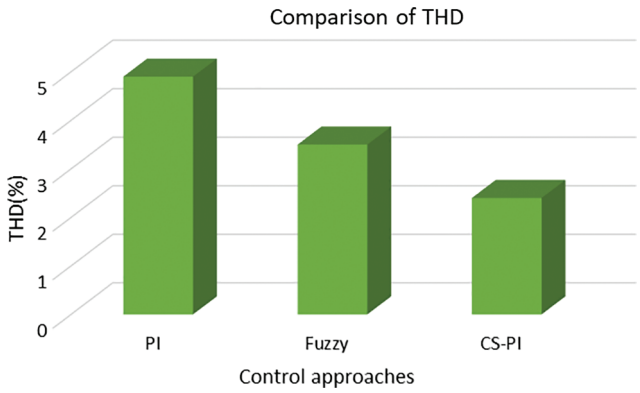
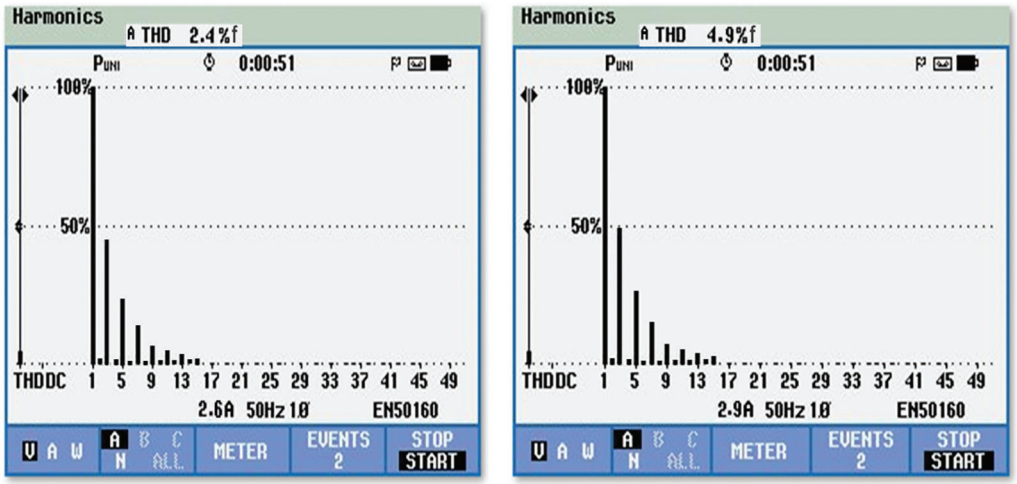


Figure 22: Comparison of THD

The THD for CS-PI and PI controller is given in Figs. 23a and 23b which reveals that the THD with CS-PI obtained is 2.4% and THD with PI controller obtained is 4.9%. On comparing both THD with CS-PI and PI, the CS-PI gives better performance indicating the efficiency of the proposed approach.



(a) (b)

Figure 23: (a) & (b) THD with CS-PI and PI controller

5 Conclusion

This proposed system examines the dynamics and efficiency of control system against fluctuations that are common in all PV panels due to variation of temperature and intensity. An improved interleaved DC-DC SEPIC converter is employed. It overcomes the drawback of high input current ripples. It also provides excellent buck boost conversion ratio. When compared to other existing converters, the proposed converter consumes lesser components and provides improved energy efficiency. A crow search algorithm is utilized for proposed converter that optimizes the parameters of PI controller. The objective of CSA optimized PI controller of proposed converter is to generate good response and enables working in Continuous Conduction Mode (CCM). The performances improved with this optimization are reduction in ripples, decrease in settling time and minimization of peak overshoots. The obtained converter outputs are applied to a 1Φ VSI which in turn converts the DC input to AC output and supplies it to the gird. After implementing CSA based PI the efficiency of proposed converter obtained is 96% and THD is found to be 2.4%. On comparing these values with existing system, the proposed system gives better performance than existing scheme. The entire behavior study of proposed work is done in MATLAB Simulink software and also the outputs are checked with hardware implementation.

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Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

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