

Genetic Algorithm Based 7-Level Step-Up Inverter with Reduced Harmonics and Switching Devices

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Abstract: This paper presents a unique voltage-raising topology for a single-phase seven-level inverter with triple output voltage gain using single input source and two switched capacitors. The output voltage has been boosted up to three times the value of input voltage by configuring the switched capacitors in series and parallel combinations which eliminates the use of additional step-up converters and transformers. The selective harmonic elimination (SHE) approach is used to remove the lower-order harmonics. The optimal switching angles for SHE is determined using the genetic algorithm. These switching angles are combined with a level-shifted pulse width modulation (PWM) technique for pulse generation, resulting in reduced total harmonic distortion (THD). A detailed comparison has been made against other relevant seven-level inverter topologies in terms of the number of switches, drivers, diodes, capacitors, and boosting facilities to emphasize the benefits of the proposed model. The proposed topology is simulated using MATLAB/SIMULINK and an experimental prototype has been developed to validate the results. The Digital Signal Processing (DSP) TMS320F2812 board is used to generate the switching pulses for the proposed technique and the experimental results concur with the simulated model outputs.

Keywords: Genetic algorithm; multilevel inverter; pulse width modulation; selective harmonic elimination; switched capacitor

1 Introduction

Multilevel Inverter (MLI) is a popular choice across industry and academia because they are well suited for medium and high-power energy conversion. MLIs produce better staircase waveform compared to two-level inverters and also possess additional benefits namely; reduction in switching losses, voltage stress (dv/dt), total harmonic distortion, and filter size which leads to wide utilization in industrial applications [1]. Most familiar conventional MLI topologies are (i) Flying Capacitor MLI (FCMLI) [2], (ii) Neutral Point Diode Clamped MLI (NPDCMLI) [3] and (iii) Cascaded H-Bridge MLI (CHBMLI) [4]. As far as NPDCMLI is concerned more numbers of switching devices are required as well as the capacitor voltage sharing is unequal, resulting in increased voltage stress across the switches [5]. In the case of FCMLI, more complex control is required because it contains more flying capacitors, which increases both the



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system's size and overall cost [6]. In the case of CHBMLI, more than one h-bridge and isolated DC sources are required to increase the output voltage levels [7–9]. CHBMLI is further classified as symmetric MLI and asymmetric MLI. Asymmetric MLI generates more output voltage levels than symmetric MLI [10,11]. Voltage boosting is essential in MLI when used in solar and electric vehicle applications. CHBMLI utilizes transformers to boost the output voltage gain, resulting in an oversized and bulkier system [12,13]. Transformer-less circuit designs were proposed as a solution to this problem by [14,15]. Although the use of a front-end DC-DC converter and energy buffer circuit eliminates the need for a transformer, the control complexity appears to be high in [14,15].

Packed U-Cell (PUC) is another evolving switched-capacitor (SC) based single input MLI topology, which is discussed in [16,17]. Despite the ability to generate the required number of output levels, the system lags in the output voltage boosting facility [16,17]. Similar to PUC, the topology with reduced device is proposed in [18]. It requires only seven switches and two diodes to produce the seven levels. Although it just requires a few devices, it falls short in terms of voltage boosting and requires three capacitors. In comparison to [18], the paper [19] exhibits improvements as it only requires eight switches and two capacitors to generate seven levels with 1.5 times the boosting factor. Using the level shifted PWM technique, the seven levels were generated with only eight switches and two capacitors [20].

Several seven-level (7L) topologies based on the three times boosting gain are presented in the following literature. In the proposed model [21], 16 switches with two capacitors are used to produce seven levels across the load. Similarly, with only 12 switches, the topology could generate seven levels of output voltage [22,23]. In comparison to [22,23], the structure only requires 11 switches to reach the required seven levels of output voltage [24]. A 7L inverter with sixteen switches and two capacitors are discussed in this study [25]. Despite the fact that this topology is capable of producing seven levels of output voltage, it necessitates the inclusion of additional switching devices. As a result, the system's overall cost shoots up. In [26], a multipurpose inverter topology has been proposed for standalone applications. Despite the fact that it can attain seven levels of output voltage, this design still necessitates 13 switches and three battery sources. The following are the benefits of the proposed inverter as stated in this paper:

- i) A single isolated DC source is sufficient for the proposed 7L inverter.
- ii) Only 11 switches and two capacitors are required.
- iii) Output voltage gain is boosted to thrice the value of input voltage (1:3) without using any additional inductor or transformer.
- iv) Sensorless control for voltage balancing across the capacitors is achieved.
- v) To minimize power loss across the switches, high-power switches are designed to operate at the fundamental frequency.

The functions of the suggested inverter are discussed in the following sections.

In Section 2, an overview of the topology and its operating modes are described.

In Section 3, the switching strategy and harmonic reduction techniques are discussed.

In Section 4, the power loss calculation has been discussed.

In Section 5, a detailed comparison has been made with various relevant topologies.

In Section 6, simulation and hardware results are described and concluded in Section 7.

2 Proposed Topology

The proposed single-phase 7L switched-capacitor based topology has been represented in Fig. 1. The proposed circuit consists of nine unidirectional and one bidirectional power semiconductor switch (a total of 11 switches). The various operating states of the suggested topology have been illustrated through the

equivalent circuits as shown in Fig. 2. It is essential to specify that the switches ST_{a1} and ST_{a3} are complementary with the switch ST_{a2} during the entire operating mode. Similarly, ST_{b1} and ST_{b3} are working inverse to the switch ST_{b2} . These complimentary switching states ensure that the switched capacitors are charged without any interruption. This charged energy is later used to elevate the load voltage gain up to thrice that of the input value. Switching pairs of $(ST_{c1}; ST_{c2})$ and $(ST_{d1}; ST_{d2})$ cannot be activated simultaneously, as this results in a short of input DC voltage source (V_{DC}). The seven different load voltage levels of $0, \pm V_{DC}, \pm 2V_{DC}$, and, $\pm 3V_{DC}$ are achieved through the various switching states as shown in Tab. 1. It is a significant constraint that during the peak level of $\pm 3V_{DC}$, the negative voltage of the input source is blocked at node t and bypassed to node r using bidirectional switch ST_{b3} .

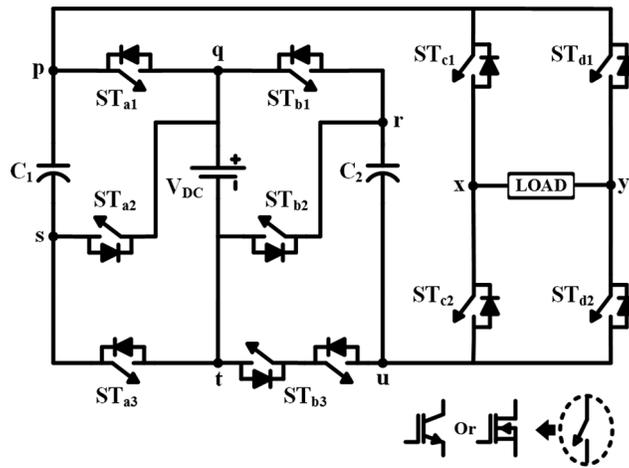


Figure 1: Proposed topology of 7 L inverter

2.1 Modeling of the Proposed Circuit

The various modes of operation can be evaluated through the derived switching model as follows. Let the dynamic function of the switches during $(k = 1, 2)$ are ST_{ak} ; ST_{bk} ; ST_{ck} and ST_{dk} respectively. The dynamic functions of the various modes can be obtained through the following equations,

$$ST_{ak} = \begin{cases} 1, & \text{if } ST_{ak} \text{ is ON,} \\ 0, & \text{if } ST_{ak} \text{ is OFF,} \end{cases} \text{ while } k = 1, 2, \quad (1)$$

$$ST_{bk} = \begin{cases} 1, & \text{if } ST_{bk} \text{ is ON,} \\ 0, & \text{if } ST_{bk} \text{ is OFF,} \end{cases} \text{ while } k = 1, 2, \quad (2)$$

$$ST_{ck} = \begin{cases} 1, & \text{if } ST_{ck} \text{ is ON,} \\ 0, & \text{if } ST_{ck} \text{ is OFF,} \end{cases} \text{ while } k = 1, 2, \quad (3)$$

$$ST_{dk} = \begin{cases} 1, & \text{if } ST_{dk} \text{ is ON,} \\ 0, & \text{if } ST_{dk} \text{ is OFF,} \end{cases} \text{ while } k = 1, 2, \quad (4)$$

The load voltage can be calculated as follows:

$$V_{xy} = (-1)^{k+1} (ST_{ck} * ST_{d(3-k)}) (V_{sq} + V_{qt} + V_{tr}) \text{ while } k = 1, 2, \quad (5)$$

where the nodes are labeled as p, q, r, s, t, u, x, and y in Fig. 1 are expressed based on the switching function values.

$$\begin{cases} V_{sq} = (1 - ST_{a1})V_{ps} \\ V_{ps} = V_{C1} \\ V_{tr} = (1 - ST_{b1})V_{ru} \\ V_{ru} = V_{C2} \\ V_{qt} = V_{DC} \end{cases} \quad (6)$$

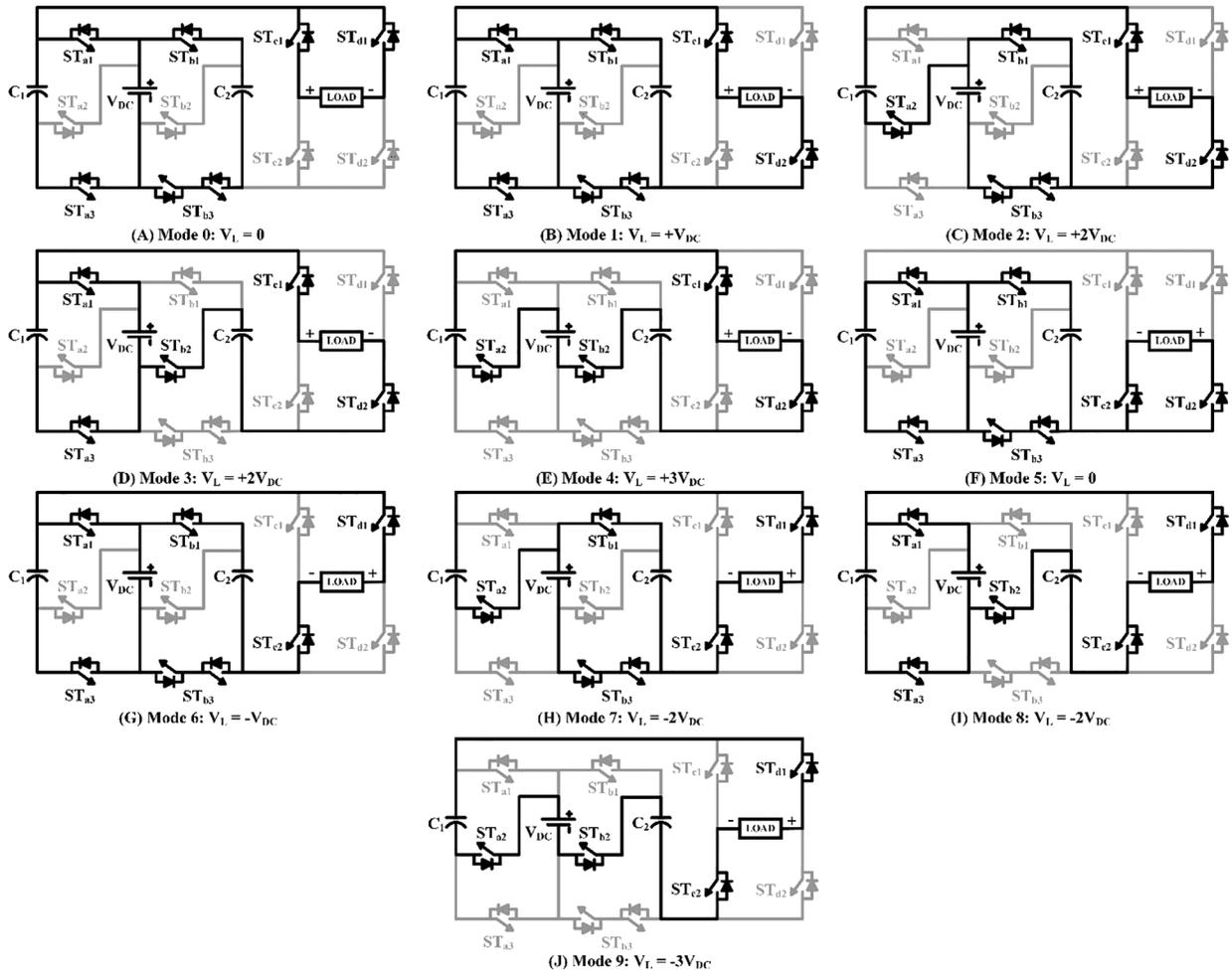


Figure 2: Various operating modes of the suggested 7 L switched-capacitor inverter

Substituting Eq. (6) in Eq. (5) returns,

$$V_{xy} = V_{out} = V_L = (-1)^{k+1} (ST_{ck} * ST_{d(3-k)}) [(1 - ST_{a1})V_{C1} + V_{DC} + (1 - ST_{b1})V_{C2}] \quad (7)$$

When $k = 1$ and $k = 2$, the output load voltage (V_{out}) is proportional to the positive and negative cycles, respectively in Eq. (7).

Table 1: Various modes and their switching states pertaining to the suggested 7 level inverter

Mode	Switching state										Capacitor state		Voltage level
	M	ST _{a1}	ST _{a2}	ST _{a3}	ST _{b1}	ST _{b2}	ST _{b3}	ST _{c1}	ST _{c2}	ST _{d1}	ST _{d2}	C ₁	
0	1	0	1	1	0	1	1	0	1	0	C	C	0
1	1	0	1	1	0	1	1	0	0	1	C	C	+V _{DC}
2	0	1	0	1	0	1	1	0	0	1	D	C	+2V _{DC}
3	1	0	1	0	1	0	1	0	0	1	C	D	+2V _{DC}
4	0	1	0	0	1	0	1	0	0	1	D	D	+3V _{DC}
5	1	0	1	1	0	1	0	1	0	1	C	C	0
6	1	0	1	1	0	1	0	1	1	0	C	C	-V _{DC}
7	0	1	0	1	0	1	0	1	1	0	D	C	-2V _{DC}
8	1	0	1	0	1	0	0	1	1	0	C	D	-2V _{DC}
9	0	1	0	0	1	0	0	1	1	0	D	D	-3V _{DC}

2.2 Operating Principle

The various switching states and operating modes of the 7L inverter are depicted in [Tab. 1](#) and in [Fig. 2](#). The charging (C) and discharging (D) states of the capacitors are represented in [Tab. 1](#).

Mode 0 ($V_{out} = 0$): In this zeroth level, as shown in [Fig. 2A](#), the switches ST_{a1}, ST_{a3}, ST_{b1}, ST_{b3}, ST_{c1} and ST_{d1} are turned on and delivers zero voltage across the load. During this mode, the two capacitors C₁ and C₂ are in charging states. With $k = 1$, the [Eq. \(7\)](#) can be written as,

$$V_{xy} = (-1)^2(0)[(1 - 1)V_{C1} + V_{DC} + (1 - 1)V_{C2}] = 0 \tag{8}$$

Mode 1 ($V_{out} = +V_{DC}$): In this first level, as shown in [Fig. 2B](#), the output voltage of (+V_{DC}) has been generated across the load by triggering the switches ST_{a1}, ST_{a3}, ST_{b1}, ST_{b3}, ST_{c1} and ST_{d2}. In this mode, the input DC source charges the capacitors voltage to V_{DC}.

$$V_{xy} = (-1)^2(1)[(1 - 1)V_{C1} + V_{DC} + (1 - 1)V_{C2}] = V_{DC} \tag{9}$$

Mode 2 ($V_{out} = +2V_{DC}$): The source voltage V_{DC} and the discharging capacitor voltage V_{C1} were combined to create the second level, as shown in [Fig. 2C](#). Furthermore, by actuating the switches ST_{a2}, ST_{b1}, ST_{b3}, ST_{c1} and ST_{d2}, the capacitor C₂ has been kept in a charging mode.

$$V_{xy} = 1(1)[(1 - 0)V_{C1} + V_{DC} + 0] = 2V_{DC} \tag{10}$$

Mode 3 ($V_{out} = +2V_{DC}$): This state has been redundant to Mode 2 as it generates (+ 2V_{DC}) voltage level by triggering the switches ST_{a1}, ST_{a3}, ST_{b2}, ST_{c1} and ST_{d2}. Capacitor C₂ discharges with V_{DC} and C₁ remains charged, as seen in [Fig. 2D](#).

$$V_{xy} = 1(1)[0 + V_{DC} + (1 - 0)V_{C2}] = 2V_{DC} \tag{11}$$

Mode 4 ($V_{out} = +3V_{DC}$): In the third level, maximum boosted voltage level of (+3V_{DC}) is obtained by connecting all the capacitors in series with the input source. In this mode, only four switches (ST_{a2}, ST_{b2}, ST_{c1} and ST_{d2}) are engaged, as shown in [Fig. 2E](#).

$$V_{xy} = 1(1)[(1 - 0)V_{C1} + V_{DC} + (1 - 0)V_{C2}] = 3V_{DC} \quad (12)$$

The switching states in mode 5 are similar to mode 0, with the exception that the ST_{c2} and ST_{d1} switches are triggered instead of the ST_{c1} and ST_{d2} switches. The switching devices in modes 6, 7, 8 and 9 are similar to those in modes 1, 2, 3 and 4 except that instead of ST_{c1} and ST_{d2} , the switches ST_{c2} and ST_{d1} are triggered.

3 Pulse Generation Strategy

The PWM strategies are employed to enhance the load voltage waveform in terms of distortion factor, lower-order harmonics, and total harmonic distortion (THD). PWM techniques are also categorized into three types based on their switching frequency: High, low, and hybrid switching frequency techniques (combination of low and high-frequency switching techniques). Some forms of high-switching frequency modulation techniques include the space vector PWM technique, carrier-based pulse width modulation technique as well as reference-based PWM technique. Low-frequency modulation technique includes fundamental frequency modulation, selective harmonic elimination PWM (SHEPWM) technique, and active harmonic elimination technique. CBPWM is classified into two types, level-shifted-carrier based PWM (LS-CBPWM) and phase-shifted-carrier based PWM (PS-CBPWM).

As illustrated in Fig. 3, the suggested inverter uses a PWM technique that combines the benefits of LS-CBPWM and SHEPWM to reduce harmonic content. In Fig. 3, the LS-CBPWM technique is demonstrated by comparing a reference sinusoidal waveform (V_{ref}) with six equal-magnitude level-shifted carrier signals (V_{cr}). The carrier signal has a higher switching frequency to eliminate the lower order harmonics. Despite the fact that the LS-CBPWM can reduce THD, the harmonic profile is dominated by 3rd and 5th order harmonics. The Selective Harmonic Elimination technique is used to substantially eliminate the 3rd and 5th order harmonics in the output voltage. The GA optimization algorithm can be used to solve the SHEPWM's nonlinear transcendental equations in order to generate the optimal switching angle [26]. The suggested seven level inverter's switching angles of $(\alpha_1, \alpha_2, \alpha_3)$ are generated by solving Eq. (18) with the constraint that α_N must be less than $\frac{\pi}{2}$. The resulting switching angles are combined with the LS-CSPWM approach to generate the required gate pulses for the 7L inverter, as shown in Fig. 5.

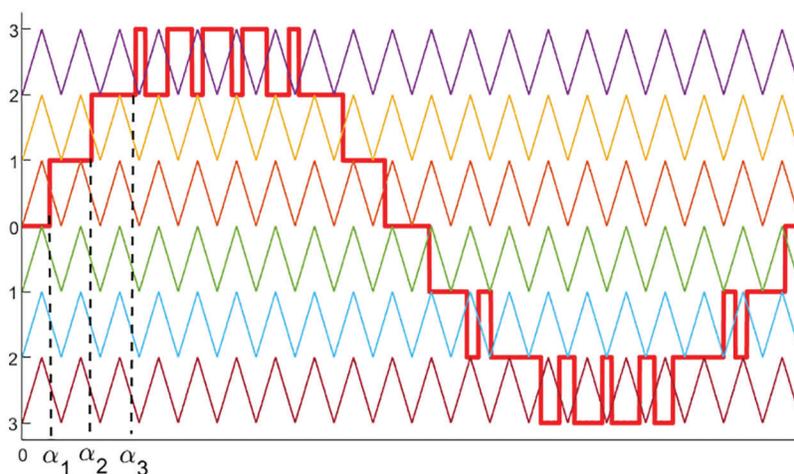


Figure 3: Pulse generation strategy for the proposed 7 L inverter

The multilevel output voltage waveform can be represented mathematically in a Fourier series, as given by,

$$V_{out(\omega t)} = \frac{4V_{dc}}{n\pi} \sum_{n=1,3,5, \dots}^{\infty} [\cos(n\alpha_1) + \cos(n\alpha_2) + \dots + \cos(n\alpha_N)] \sin(n\omega t) \quad (13)$$

The peak voltage of each n^{th} harmonic component is provided by,

$$V_h = \frac{4V_{dc}}{n\pi} [\cos(n\alpha_1) + \cos(n\alpha_2) + \dots + \cos(n\alpha_N)], \quad n = \text{odd} \quad (14)$$

Eq. (14) can be used to compute the fundamental (V_1) peak voltage as well as the 3rd and 5th order values.

$$\begin{cases} n = 1 : V_1 = \frac{4V_{dc}}{n\pi} [\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3)] \\ n = 3 : 0 = [\cos(3\alpha_1) + \cos(3\alpha_2) + \cos(3\alpha_3)] \\ n = 5 : 0 = [\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3)] \end{cases} \quad (15)$$

Considering N switched sources, SHEPWM can minimize harmonics up to $2N-1$. The inverter's modulation index can be calculated by,

$$M = \frac{\pi V_1}{4N * V_{dc}}, \quad 0 \leq M \leq 1 \quad (16)$$

The modulation index with respect to number of levels can be derived as,

$$M = \frac{1}{3} \sum_{i=1,2, \dots}^{N_{Level} - 1} 2 \cos(\alpha_i), \quad 0 \leq M \leq 1 \quad (17)$$

where $0 < \alpha_1 < \alpha_2 < \dots < \alpha_N < \frac{\pi}{2}$

GA's main purpose is to reduce the harmonic value to the smallest possible value, and the firing angles are also chosen by a genetic algorithm. The fitness function is represented as,

$$\text{Fitness function} = \left(100 \frac{V_1^* - V_1}{V_1^*}\right)^4 + \sum_{n=3,5, \dots}^{2N_{Level}-1} \frac{1}{n} \left(50 \frac{V_n}{V_1}\right)^2 \quad (18)$$

where V_1^* is the required peak of the fundamental component and it can be determined by the modulation index. The switching angles for various modulation index values are shown in Fig. 4a. Furthermore, the optimum switching angle is reached when the modulation index value is 0.8. The 3rd and 5th order harmonic percentages for various modulation index values are shown in Fig. 4b. Among the available modulation indexes, Fig. 4b displays the region with the least THD. As illustrated in Fig. 5, the capacitor voltage is stabilized by employing the voltage balancing algorithm technique between the C_1 and C_2 capacitors. The two C_1 and C_2 switched capacitors are charged to the DC source voltage level. Tab. 1 exhibits the charging and discharging of the proposed inverter. Furthermore, C_1 and C_2 capacitors are kept at charging mode during the 0 and $\pm V_{DC}$ voltage levels and discharged during the $\pm 3V_{DC}$ voltage level. Furthermore, the C_1 and C_2 capacitors are charged during the 0 and $\pm V_{DC}$ voltage levels, and discharged during the $\pm 2V_{DC}$ and $\pm 3V_{DC}$ voltage levels.

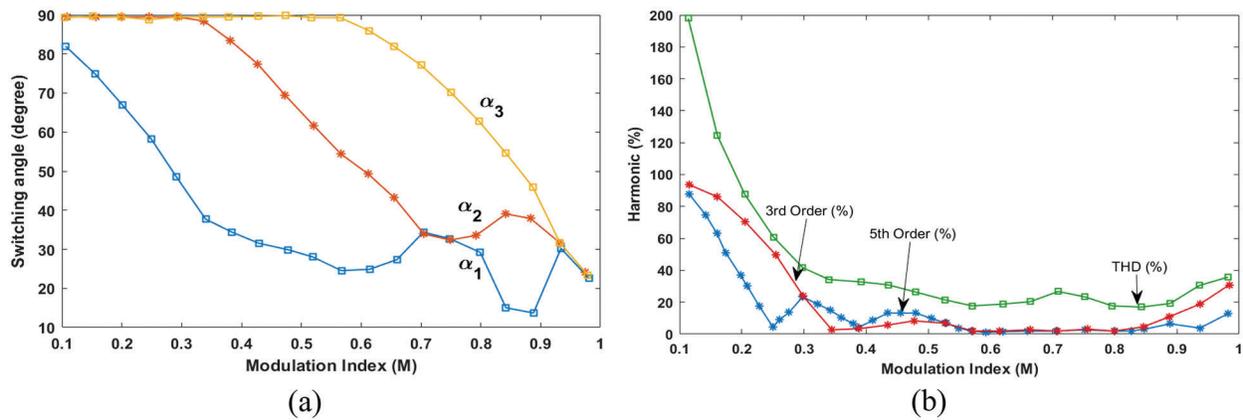


Figure 4: GA optimization results in terms of modulation index vs. (a) switching angle selection and (b) harmonic values

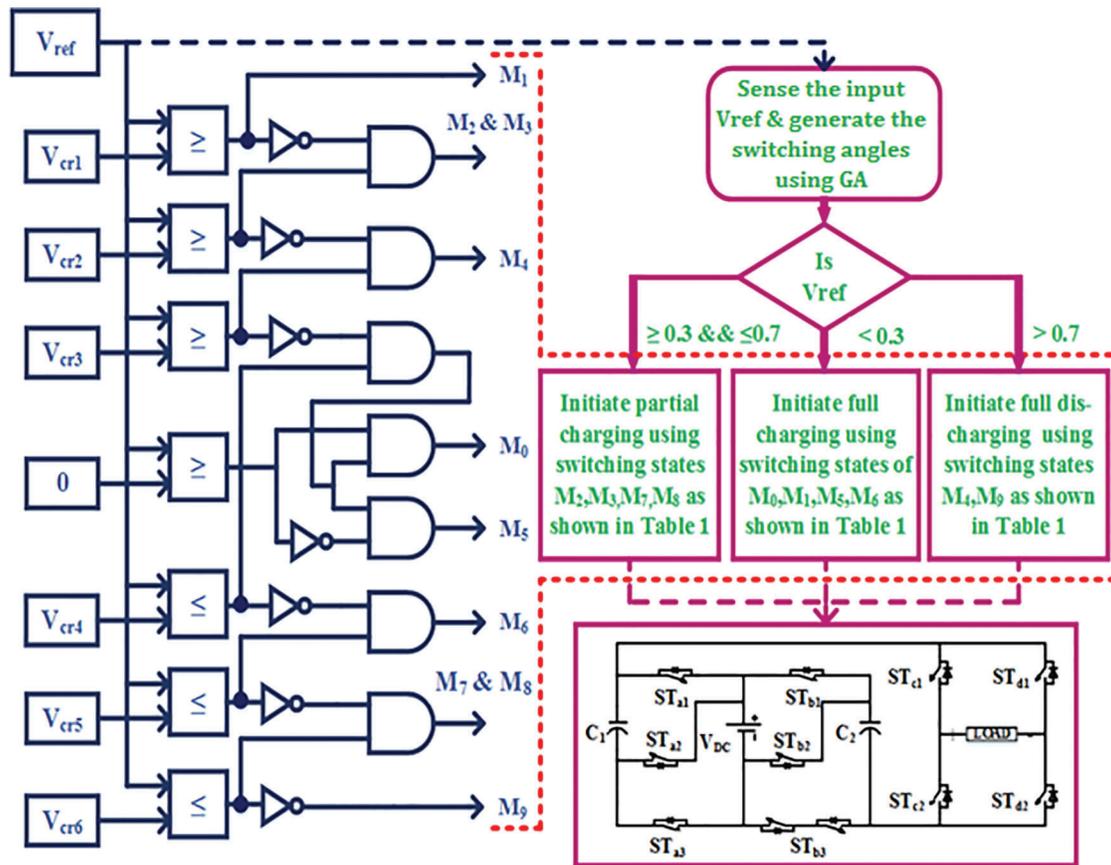


Figure 5: Self-balancing capacitor voltage algorithm with Genetic Algorithm

4 Power Loss Calculation

4.1 Conduction Losses (P_{cl})

The conduction loss (P_{cl}) appears during the on-state of the power semiconductor switches, and mainly due to its internal resistance R_{in} . The (P_{cl}) can be calculated by

$$P_{cl} = \sum_{j=0}^{10} R_{in} I_{out}^2 \quad (19)$$

where I_{out} is the magnitude of the output current flows through the j^{th} power switch.

4.2 Switching Losses (P_{sw})

The switching loss is caused by the overlap of current and voltage across the switches during the transition of switching states, i.e., from ON to OFF state, it is called as turn-on power loss ($P_{swl, ON}$) and from OFF to ON state called as a turn-off power loss ($P_{swl, OFF}$). In addition, these states have significant values in voltage and current magnitude, leading to switching power loss (P_{swl}).

$$P_{sw,ON} = f_s \int_0^{t_{on}} v(t)i(t)dt = f_s \int_0^{t_{on}} \left(\frac{-V_{Bl}(t - t_{on})}{t_{on}} \right) \left(\frac{I_{out}}{t_{on}} t \right) dt = \frac{1}{6} f_s V_{Bl} I_{out} t_{on} \quad (20)$$

$$P_{sw,OFF} = f_s \int_0^{t_{off}} v(t)i(t)dt = f_s \int_0^{t_{off}} \left(\frac{-V_{Bl}(t - t_{off})}{t_{off}} \right) \left(\frac{I_{out}}{t_{off}} t \right) dt = \frac{1}{6} f_s V_{Bl} I_{out} t_{off} \quad (21)$$

The switching power loss can be calculated using Eqs. (20) and (21)

$$P_{sw} = P_{sw,ON} + P_{sw,OFF} = \sum_{j=0}^{11} \frac{1}{6} f_{sj} V_{Blj} I_{out} t_{on+off} \quad (22)$$

In the Eq. (22) f_{sj} , V_{Blj} , t_{on} and t_{off} is the switching frequency, blocking voltage and on-time and off-time of the of j^{th} switch respectively.

4.3 Ripple Losses (P_{ripl})

Due to the capacitor equivalent series resistance (r_{ESR}) a voltage drop (V_{cd}) appears occurs across the capacitor. The ripple loss can be derived for any value of capacitance (C_p) is as follows

$$P_{ripl} = \frac{f_s}{2} * C_p * V_{cd} \quad (23)$$

Eventually, using Eqs. (19), (22) and (23), the total power loss (P_{loss}) and efficiency (η) of the proposed inverter are calculated as,

$$P_{loss} = P_{cl} + P_{sw} + P_{ripl} \quad (24)$$

$$\eta = \frac{P_{out}}{P_{in}} * 100, \text{ where } P_{in} = P_{out} + P_{loss} \quad (25)$$

where, P_{in} and P_{out} are the input and output powers of the inverter.

5 Comparative Studies

The advantages of the proposed system are demonstrated by contrasting it with other known conventional and related topologies. Tab. 2 shows a detailed comparison of the proposed model to other configurations in terms of total number of switches (N_{sw}), drivers (N_{driver}), diodes (N_{diode}), capacitors (N_{cap}), DC source (N_{DCS}), switching devices (N_{device}), output voltage levels (N_{Level}), voltage stress (V_{stress}), gain ratio (G) and boosting facility. The comparison in Tab. 2 reveals that traditional topologies use more switching devices and have significant lag in the boosting facility. Topologies with triple times

voltage boosting factors are described in this literature [14] and [21–25]. Even though, these topologies are identical in the number of output levels and gain they lag mostly in device count. The topology in [14] requires 13 switches, 4 diodes, and a total of 30 semiconductor devices. In comparison to the proposed model, the topology necessitates the use of more switches and diodes. The topology in [21] demands 16 switches and 14 gate driver circuits, a higher device count that results in higher power loss and cost. In [22,23], voltage stress across the switches is reduced to $2V_{dc}$ and requires only 12 switches. However, compared to the proposed model the total device count is higher. In [24], only 11 switches are required to generate 7 levels across the load, but three numbers of capacitors are required, resulting in control complexity. Topology [25] necessitates 5 additional switches than the proposed topology, resulting in increased cost and size. The device comparison in Fig. 6a illustrates that the proposed model only requires 11 switches and 10 gate driver circuits to generate the required 7L, which is significantly less than other topologies. Furthermore, the proposed model only requires two capacitors, resulting in a significant reduction in total cost and inverter size, as shown in Fig. 6b.

Table 2: Device comparison of 7L proposed inverter with other topologies

Topology	N_{Level}	G	N_{sw}	N_{driver}	N_{diode}	N_{device}	N_{DCS}	N_{Cap}	A/ N_{Level}	A/G	V_{Stress}	Boosting facility
CHBMLI	7	1	12	12	Nil	24	3	Nil	3.9	27	V_{dc}	NO
NPDCMLI	7	1	12	12	10	34	6	6	6.6	46	V_{dc}	NO
FCMLI	7	1	12	12	Nil	24	1	7	4.6	32	V_{dc}	NO
[14]	7	3	13	13	4	30	1	3	4.9	11.3	V_{dc}	YES
[21]	7	3	16	14	Nil	30	1	2	4.7	11	$3V_{dc}$	YES
[22]	7	3	12	12	Nil	24	1	2	3.9	9	$2V_{dc}$	YES
[23]	7	3	12	11	Nil	23	1	2	3.7	8.7	$2V_{dc}$	YES
[24]	7	3	11	11	1	23	1	3	3.9	9	$3V_{dc}$	YES
[25]	7	3	16	14	0	30	1	2	4.7	11	V_{dc}	YES
Proposed	7	3	11	10	Nil	21	1	2	3.4	8	$3V_{dc}$	YES

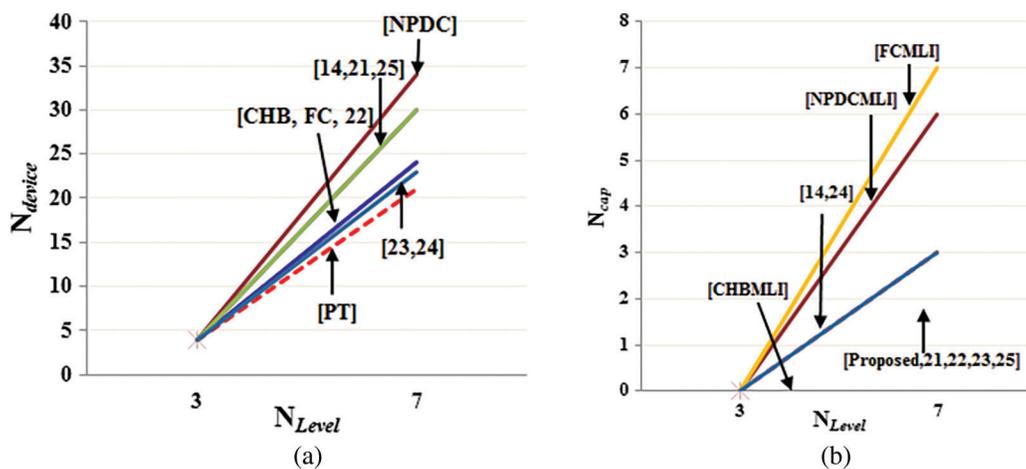


Figure 6: Comparison of output voltage levels with respect to (a) the total number of switching devices and (b) total number of capacitors

As seen in Fig. 7a, the total component per gain ratio (A/G) is also lesser in the suggested model than in other topologies.

$$\frac{A}{G} = \frac{N_{sw} + N_{driver} + N_{diode} + N_{DCS} + N_{cap}}{G} \tag{26}$$

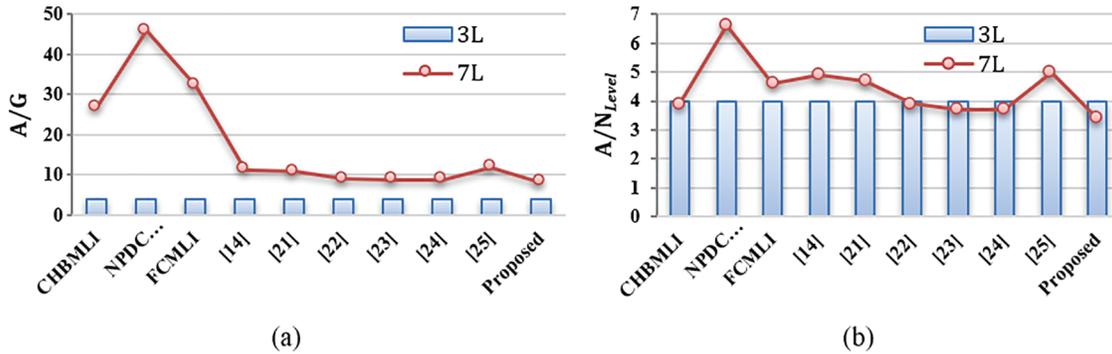


Figure 7: Comparison of required components with (a) gain factor and (b) per level factor

Similarly, as shown in Fig. 7b, the total component per level (A/N_{Level}) in the suggested structure is lesser than in other topologies.

$$\frac{A}{N_{Level}} = \frac{N_{sw} + N_{driver} + N_{diode} + N_{DCS} + N_{cap}}{N_{Level}} \tag{27}$$

5.1 Extension of the Proposed 7L Inverter

The cascaded arrangement of the suggested 7-level structure has been designed to produce the higher output voltage level, as illustrated in Fig. 8. N cascaded modules make up the structure. The proposed 7-level inverter topology is used in each module.

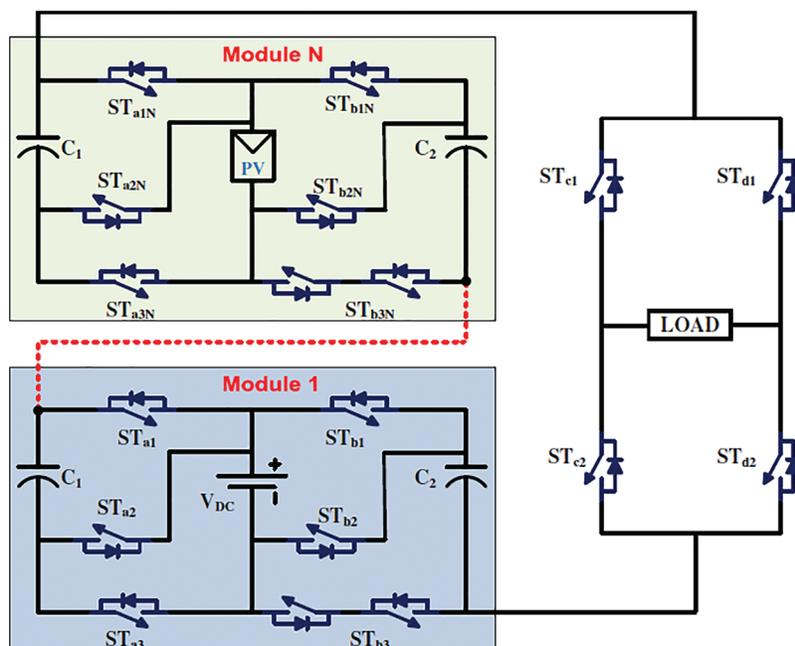


Figure 8: Proposed 7 L topology in a cascaded arrangement

Using $(7N + 4)$ switches, $2N$ capacitors, and N input DC sources, the suggested structure can achieve $(6N + 1)$ output voltage levels when all modules have the same magnitude of DC voltage sources. To replace the DC source, existing renewable resources such as photovoltaic (PV), fuel cell, and others can be employed. The advantage of the cascaded configuration is that it requires only one H-bridge for polarity switching, while the remaining modules are employed for voltage boosting.

6 Simulation and Hardware Prototype Results

The prototypical 7L inverter model has been designed and analyzed with the help of SIMULINK tool in terms of static and dynamic characteristics. The model has been tested with the load value of 2 kW at 0.8 lagging power factor and the simulated results are displayed in Fig. 9. The inverter delivers peak ac output voltage value of 300 V, fed from a 100 V DC source. Fig. 9 displays the waveform of output load voltage (V_{out}), current (I_{out}) and capacitor voltages (V_{C1} and V_{C2}) for the connected load value of ($R = 50 \Omega$ and $RL = 40 \Omega + 100 \text{ mH}$). Thus, the simulated results ensure that the proposed model has thrice voltage boosting capability without adding additional components. Also, the two capacitor voltages are maintained constant around 100 V during charging and reduced up to 94 V during peak discharging for a load of 2 kW. This shows that the capacitor ripple voltage is lesser and hence it enhances the durability of the capacitor.

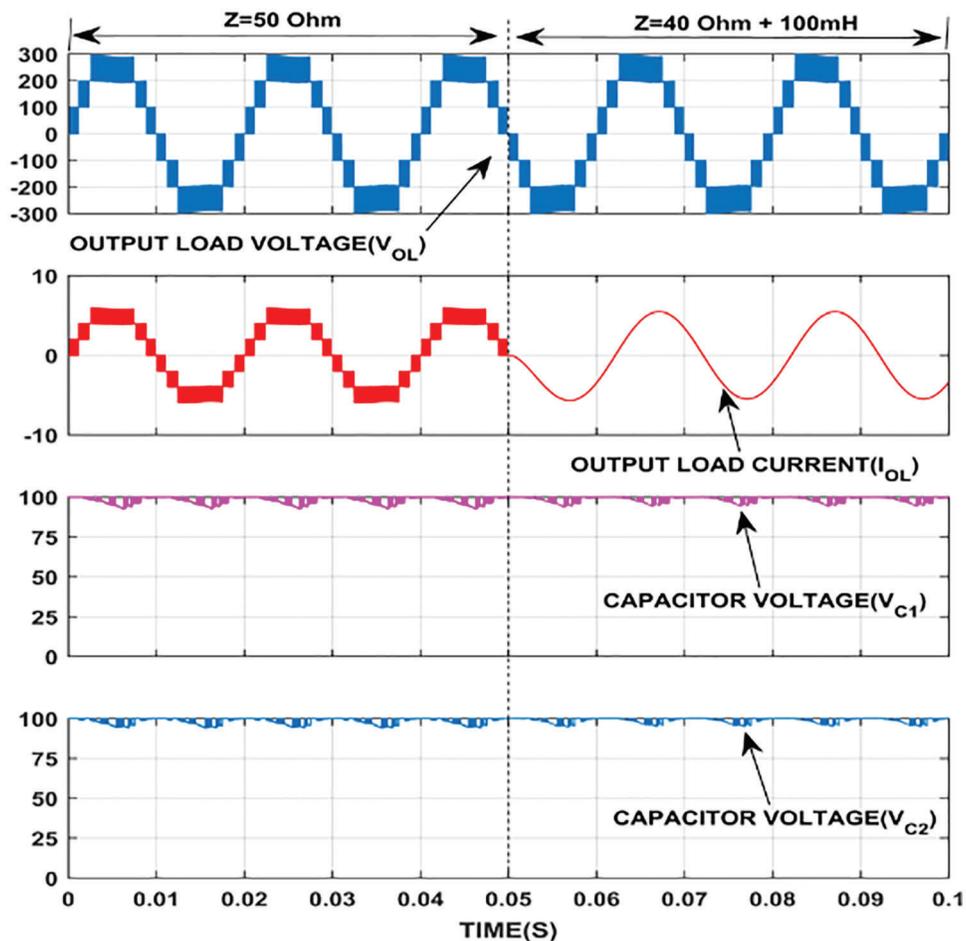


Figure 9: Simulated output waveform of the 7 L inverter with $R = 50 \Omega$ and $RL = 40 \Omega + 100 \text{ mH}$

The THD profiles of the proposed inverter can be seen in Fig. 10. Compared to the LS-CBPWM, the combined (SHE and LS-CB) PWM approach exhibits lower voltage harmonics by 19.62%. The lower order harmonics of 3rd and 5th are eliminated due to the influence of optimal switching angle generated through genetic algorithm.

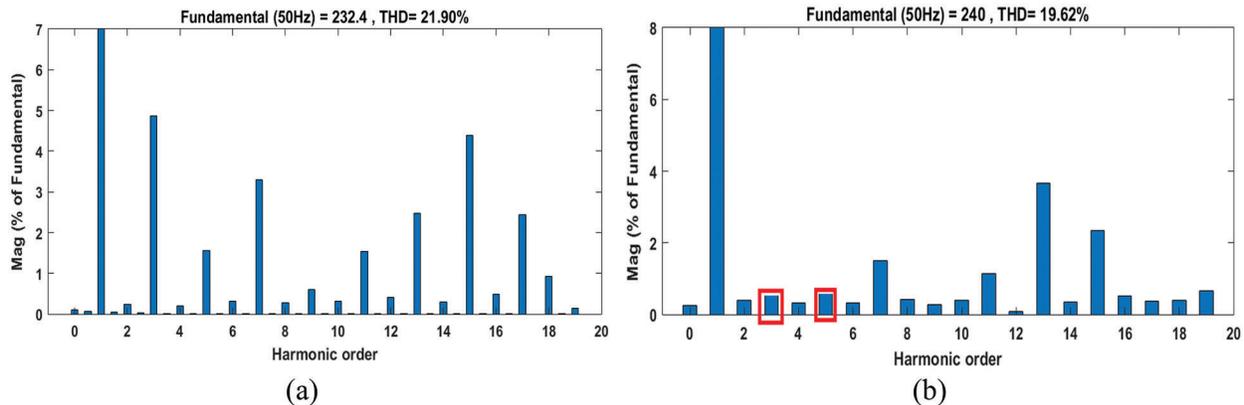


Figure 10: THD analysis (a) without SHEPWM (b) with SHEPWM reduced 3rd and 5th order

The dynamic load changing characteristics of the proposed model has been verified with two different values of loads ($Z = 50 \Omega$ and $Z = 40 \Omega + 100 \text{ mH}$) and is displayed in Fig. 9. It has been observed that the V_{out} waveform remains unaltered and the shape of the output current waveform alone changes due to inductive load change. Moreover, the change in load from $Z = 50 \Omega$ to $Z = 40 \Omega + 100 \text{ mH}$ has reduced the ripple content across the capacitor voltage. The proposed 7-level inverter has been validated using a hardware archetype is shown in Fig. 11. TMS320F2812 module has been used to provide gate signals for the driver ICs. The switching algorithm is encoded in TMS320F2812 processor using code composer studio (CCS) software.

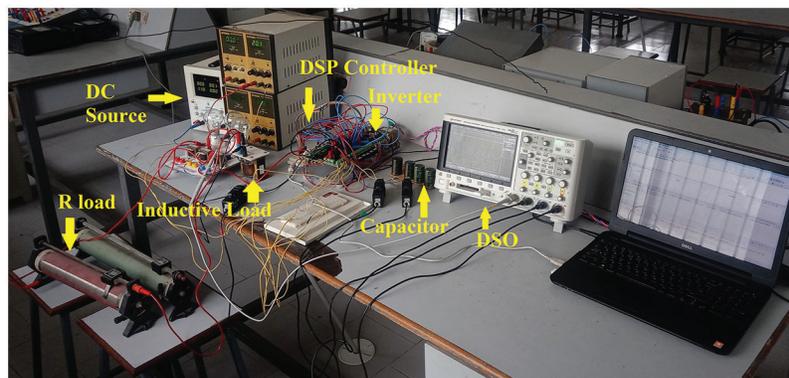


Figure 11: Hardware prototype

Tab. 3 presents the test evaluation parameters of the designed 7L single phase inverter prototype. The proposed model's output load current and voltage waveforms are examined using a key sight DSO oscilloscope. The fluke meter is used to determine the load's overall harmonic profile. The prototype is tested with a 90 V DC input, and the resulting capacitor voltage, load voltage, and current are shown in Fig. 12a. The seven voltage levels of ($\pm 90 \text{ V}$, $\pm 180 \text{ V}$, $\pm 270 \text{ V}$, 0 V) with a 5 A output current can be

seen in Fig. 12a. The enlarged waveform of the prototype results with the current values of the capacitor is shown in Fig. 12b.

Table 3: Prototype test parameters

Parameter	Value
DC input source	100 V
Capacitor	2200 μ F
Load Frequency	50 Hz
Switching Frequency	2.5 kHz
Switches	IRFP350
Gate Driver	HCPL250
Controller	TMS320F2812

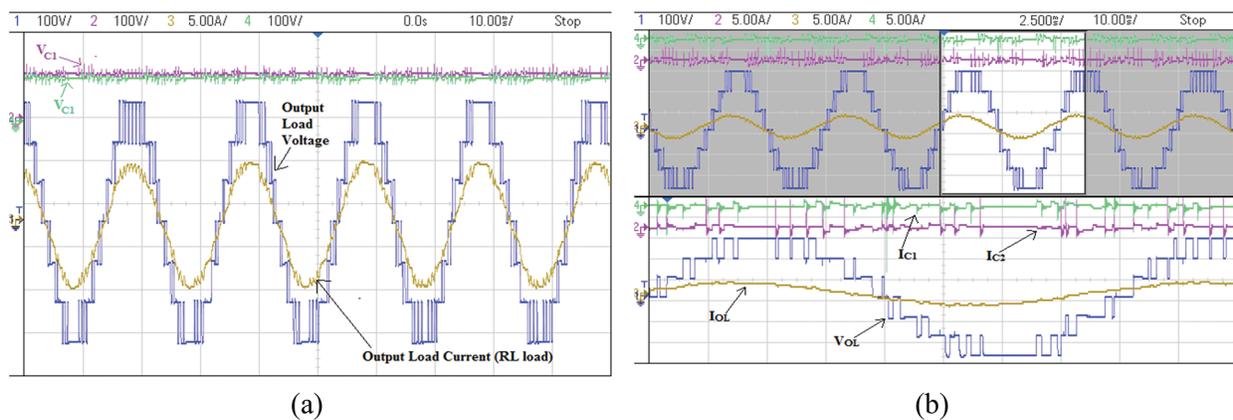


Figure 12: Experimental results; (a) RL load $Z = 40 \Omega + 100 \text{ mH}$ with capacitor voltage and (b) RL load $Z = 40 \Omega + 100 \text{ mH}$ with capacitor current in magnified waveform

Furthermore, the prototype characteristics are evaluated using Fluke 430-II meter and the test results of the 7 L inverter are shown in Fig. 13. The prototype is tested with an 85 V DC input voltage and a $Z = 40 \Omega + 100 \text{ mH}$ RL load. Output voltage and current waveforms are shown in Fig. 13a. The THD value is around 21% as shown in Fig. 13b, which is slightly higher than the simulated value. The both the capacitor voltage of V_{C1} and V_{C2} are shown in Figs. 13c and 13d respectively. Both the capacitors C_1 and C_2 maintain its voltage around 83 V. It shows that the self-balancing voltage technique provides better stability during peak loads. Thus, the prototype validates the simulated results.

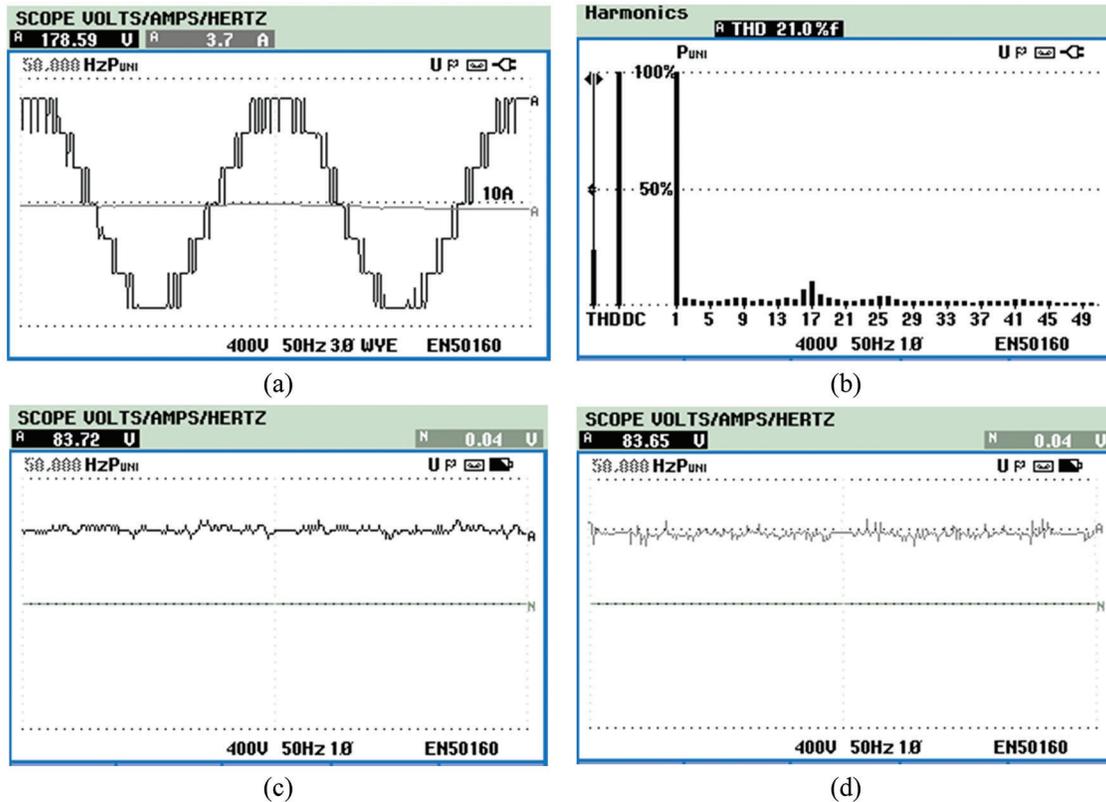


Figure 13: Experimental results in fluke meter: (a) Load voltage and current, (b) Total Harmonic Distortion (THD) (c) Capacitor voltage (V_{C1}) and (d) Capacitor voltage (V_{C2})

7 Conclusion

A single DC sourced seven-level inverter using switched capacitor technique is proposed in this paper. The highlight of the proposed model lies in boosting the output voltage into three times that of input voltage. Inherently, with the use of two switched capacitors it could generate seven voltage levels with the minimum quantity of power switching devices and gate control circuits. The GA algorithm based SHEPWM has been used to eliminate the 3rd and 5th order harmonics. Similarly, the suggested inverter exhibits the advantage of self-balancing algorithm, which retains the capacitor voltage during vigorous load changes. Mathematical modeling for the various operating states with power loss calculation is described in this paper. A detailed comparative analysis, made with the relevant level generating MLIs reveals that proposed model has better boosting capability with reduced switching devices and voltage stress across the switches. The simulated results of the proposed inverter are validated through the experimental prototype which confirms its suitability for single isolated DC to AC conversion system.

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